Auxiliary PLD U2:
- Common serial lines: SDL, SDO, SCLK.
- DAC_CS[0:8]: Chip Select for the voltage DACs
- ADC_CS[0:16]: Chip Select for the telemetry ADCs
- MUX[K[0:3]] and MUX[R[0:3]]: control lines for the clock signals multiplexers
- Output enable lines.

Auxiliary PLD U3:
- Digital clocks: CLK[0:31]
- Fast biases data: FIBAS_D[0:31]
- Fast biases control (SLEEP, WRT, CLK)
connections to VIO pins on J1 and J2 need additional consideration so as not to short the +3.3 and +5 together sometime in the future.

P1 and P2 provide +5V and +3.3V digital and some +/-12V

P3 provides +5V analog +/-15V analog

+/- some high voltage, say 40V analog grid HV grid