MONSOON
Clock and Bias Board
Test Procedures

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Revision: 2.0

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## Revision History

<table>
<thead>
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<th>Version</th>
<th>Date Approved</th>
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</tr>
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<td>0</td>
<td>3/31/2006</td>
<td>All</td>
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<tr>
<td>1.0</td>
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</tr>
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1.0 Introduction

This document covers the testing strategy for the MONSOON Clock and Bias Board to take the board from post-manufacture to a fully functional state. All tests described in this document pertain to the latest hardware revision level of the subject board. The tests described here do not prove that the board under test will meet specification but will test the full functionality of the board and identify failures that may result from component and manufacture problems. The test assumes the tester is familiar with the use of the MONSOON Engineering Console (MEC) and can execute the required commands. The tests are divided into progressive stages ranging from 1 to 8. Each higher number stage uses assumptions of the board condition that requires the successful completion of the previous stages. The test sequence is highly automated but the tester must be able to discern whether the various readings presented are reasonable. Read the instructions for each test step to aid in this process.

In the description for these tests, certain conventions are followed to ease comprehension. These conventions and examples of each are presented in Table 1.

Table 1 - Test Description Conventions

<table>
<thead>
<tr>
<th>Convention</th>
<th>Example</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linux commands that are typed on a Pixel Acquisition Node (PAN) xterm window</td>
<td>mecStart</td>
<td><strong>Boldface characters</strong></td>
</tr>
<tr>
<td>Commands typed to the mec command line</td>
<td>ppxSetAVP</td>
<td><strong>Boldface italics</strong></td>
</tr>
<tr>
<td>Buttons on the Detector Head Electronics (DHE) boards or MEC</td>
<td>&gt;startExp&lt;</td>
<td><strong>Bold italics</strong> &lt;br&gt; <strong>underlined inside &gt; &lt; symbols</strong></td>
</tr>
<tr>
<td>Designate data values that are returned in the PAN xterm or mec console window</td>
<td>dir</td>
<td><strong>Italics</strong></td>
</tr>
<tr>
<td>Responses from the programs</td>
<td>this is a response</td>
<td><strong>Courier font</strong></td>
</tr>
<tr>
<td>Specific board signal names</td>
<td>FBIAS1</td>
<td><strong>BOLDFACE SMALL CAPITALS</strong></td>
</tr>
<tr>
<td>MEC attribute names</td>
<td>mcbCodeID</td>
<td><strong>Boldface italics</strong></td>
</tr>
</tbody>
</table>

The result of each test will be a test report generated by the tester and the MEC in a file called MNSN_EL_10_0300SNnnnn_vvv.btr (where SNnnnn is the serial number and vvv is the test sequence number for this board). This file should be copied to the relevant area of the MONSOON archive in the following directory:

/MNSN/MonsoonAdmin/Production/TST_Repository/TSTResults/

This file is a record of the test and an analysis of the test results that can be printed out and kept in the system binder supplied to the end user. The test procedure functions will request the entry of data as required.
1.1 Required Equipment

- DHE with programmable power supplies and 8- or 6-slot backplane chassis. For the Clock and Bias Board test, three power supplies are required; Digital, ±5V Analog and ±15V Analog.

- Clock and Bias transition board with ribbon cables to run from the transition board to the breakout box.

- Personal Computer running MS Windows 2000 or Windows XP. The PC must be connected to the network with the \big-boy\MNSN disk mapped into the Windows disk structure. Required programs are Word and Xilinx Impact. A second LINUX PC with a Systran board installed is required to run the MONSOON Engineering Console (MEC) software.

- JTAG-programming cable.

- Agilent 54622D Oscilloscope, Agilent 34970A Data Acquisition Unit, HP 974A digital multimeter and signal breakout box. See Figure 4 for a photograph of a typical breakout box.

- Rainbow ribbon cable to run from the breakout box to the Agilent 34970A Data Acquisition Unit.

1.2 Test Schedule

Stage 1. Preparation of documentation

   Step i. See Figure 1 for board serial number location.

   Step ii. Create a new Assembly Record Tag (ART) for the board. If the circuit board was previously inspected or tested, an ART will accompany it. The ART is a record of every action that has been taken on the board. If an ART is required, send an e-mail request to:

   mailto:dstover@noao.edu
Step iii. Using a comparison photograph, visually inspect the board for physical damage, missing and misplaced components. See Figures 2 and 2A.
Stage 2. Configure Board Firmware and Power Supplies

Step i. Install the jumper configuration required by the system. Jumper configurations depend on the users’ requirements. Note the jumper configuration as locations will be entered into the Board Test Record file. Jumper pins and functions are listed in the following table. See Figures 3 and 3A for typical jumper locations.

Table 2 – Jumper Configuration

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Pins</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP1</td>
<td>2 and 3</td>
<td>BIAS VREF1</td>
</tr>
<tr>
<td>JP2</td>
<td>1 and 2</td>
<td>FBIAS VREF</td>
</tr>
<tr>
<td>JP3</td>
<td>2 and 3</td>
<td>BIAS VREF0</td>
</tr>
<tr>
<td>JP4</td>
<td>2 and 3</td>
<td>CLK VREF2</td>
</tr>
<tr>
<td>JP5</td>
<td>2 and 3</td>
<td>CLK VREF0</td>
</tr>
<tr>
<td>JP6</td>
<td>2 and 3</td>
<td>CLK VREF1</td>
</tr>
<tr>
<td>JP7 and JP8</td>
<td>Shorted</td>
<td>GND</td>
</tr>
<tr>
<td>JP9</td>
<td>1 and 2</td>
<td>SUPPLY SLCT</td>
</tr>
<tr>
<td>JP10</td>
<td>Open</td>
<td>3.3v LOCAL GEN</td>
</tr>
<tr>
<td>JP11</td>
<td>Shorted</td>
<td>LOCAL OSC ENBL</td>
</tr>
</tbody>
</table>

Clock and Bias Board JP1, JP2 and JP3
Figure 3
Step ii. Locate a test backplane, suitable power supplies and a PAN computer. Inspect the backplane for bent pins and fit the appropriate test transition card in slot 6. Set the power supply voltages and overcurrent limits to those listed in Table 5 in Appendix II.

**NOTE:** The results of most test stages will be filled in automatically by the testing software. Some stages require the test operator to take readings and record them in the test program.
Stage 3. Mechanical Fit, Power Consumption and Firmware Programming Tests

NOTE: In this and subsequent stages, readings will be taken on the circuit board, at the power supplies and the breakout box. The testing program indicates what test points to use for each test. Figure 4 shows a typical breakout box.

![Breakout Box](image)

**Figure 4**

Step i. With the power to the chassis off, carefully insert the new Clock and Bias board for the first time in slot 6. While inserting the board, check for the alignment of the connectors and key.

Connect a JTAG programming cable to the JTAG port and the programming pod. See Figure 5.

Remove Master Control Board (MCB) from the system backplane.

Step ii. Apply power to the board in the following order: 5V Digital, ±5V Analog, then ±15V Analog. Compare the static power supply consumption with that noted in Table 5 of Appendix II.

Note that the “Status” LED illuminates at this time.
Step iii. Now follow the procedures outlined in Appendix I to load the field programmable devices.

Step iv. Once programming of the FPDs is complete, re-insert Master Control Board (MCB) into the chassis.

Connect the J2 connector from the Clock and Bias Transition Board to P2 on the breakout box.

Connect the J3 connector from the Clock and Bias Transition Board to P3 on the Breakout Box.

Connect the rainbow ribbon cable to “Bias’s” on the Breakout Box.

Connect the green oscilloscope lead to the GND bus pins on the Breakout Box. Then, connect the other measuring lead to the BIASOUT0 pin of the P3 Slow Bias Outputs bank.

Power up the Data Acquisition unit and the Oscilloscope.

Re-apply power to the chassis and compare the power supply consumption with that noted in Table 6 in Appendix II.

Step v. Press \texttt{>RESET<} on the front of the Clock and Bias board and note that the front panel “Status” LED (D1) turns off and turns back on when the \texttt{>RESET<} button is released. This tests local reset and FPGA boot functions.
Step vi. Open two xterm windows on the PAN. In the first xterm window, type `fs0` and look at the fiber link status. The status will probably show data in the receive FIFO buffer and should show the DHE to be in reset mode by having the `dir`(ection) bit true in the IO register (NR.D.P2.P1.S: \(i=0_{1x0}\)). The status command should return something similar to the following:

```
FibreXtreme (SL) Monitor (sl_mon) rev. 3.02 (2003/10/06)
Driver:  rev. b2-835455:776764 for Linux with API rev. 2.1
Hardware: unit/bus/slot 0/1/4 - SL100 (D64) Firm. 1C.13 (1C.13)
for 5.0V PCI
  Link Control Register  (CSR 0x08) = 0x37
  Link Status Register  (CSR 0x0c) = 0x200 Link is UP
  FPDP Flags Register   (CSR 0x10) = 0x200 NR.D.P2.P1.S:
i=01110 o=00000
  FIFO Threshold Register (CSR 0x14) = 0x0 Int.thr. = 0x0
  Data count    = 0xE75D (59229) bytes
  Link (and other) Errors = 3
Configurable parameters:
  Loop Configuration:   0   (Point-to-Point)
  Max Timeout:          600000 (6000000 ms)
  Flow Control:         0 (NO) Halt on link error:   1
                      (YES)
```

Use the command `fc0` to clear the read buffer. Repeat the `fc0` command until the read FIFO buffer is empty (0:0 Bytes).

Stepvii. In the other xterm window, start the PAN software and MEC using the command:

```
runBoardTest clk
```

The four PAN process windows and the MEC window will be displayed as shown in Figure 8.
Figure 8

PAN and MEC Windows

Doc. File: MNSN-TS-01-0004 CBB Testing R2
Doc. Number MNSN-TS-01-0004 R2.0

Created on 11/9/2009
Step viii. Verify that the text fields
“Step 1. Enter Host Name” and
“Step 2. Port Number”
contain the correct PAN machine name and port number (5142). If these items are not filled in, enter the correct information.

Press the >STEP 3. CONNECT< button on the MEC. The ATTRIBUTE CATEGORIES page will appear.

Step ix. Next press the >RESET< then the >ASYNCResp< buttons on the MEC. Synchronization of the communication link will occur. Verify the “PIX” and “SEQ” LEDs on the MCB are turned off.

Step x. Press the >SYSTEM SETUP< button and execute “Step 5.”

In the Configuration Files window press the >MAJOR MODE LOAD< button. Click on the ATTRIBUTE CATEGORIES screen.

Press >ENVIRONMENT< and >UPDATE<. See Figures 9 and 10.

![Configuration Files Window](Figure 9)
Step xi. In the Configuration Files window (Figure 8), press **SEQUENCER SETUP LOAD** and **MAJOR MODE LOAD** again. This will load the board-specific test routines for the Clock and Bias board.

Step xii. Press **UPDATE** in the Environment Attributes page of the Attributes Categories window.

Verify the “Status” LED on the CBB is turned off.

**Stage 2.** Configure board firmware and check power supplies.

Step i. Press **LOAD BOARD TEST** button on the MEC. The available test frames are displayed. See Figure 11.
Step ii. Press >LOAD TEST FRAME< for the Clock and Bias Board Test. The CBB testing panel will be displayed as shown in Figure 12.

![CBB Testing Panel](image)

CBB Testing Panel
Figure 12

Step iii. Enter name, date, board serial number and test sequence number in the Testing Panel window. If a board is being tested for the FIRST time, enter 1. (Enter a new sequential number for each successive test performed on the same board.)

**CAUTION:** When entering data, ensure that it is entered correctly. Typographic errors, such as misplaced decimal points or dashes, will cause incorrect calculations in subsequent stages. Unusable test results will be the outcome.

To enter information into the Test Data File Path field, a new directory folder must be manually created for the board being tested using a separate xterm window. This folder must be named according to the serial number of the board.

**Example:** sn012

Create the new folder in the following location:

```
//home/monsoon/BoardTests/clkBiasBrdTest/
```

Enter the complete location path, including newly created folder, in the Test Data File Path field of the Testing Panel window.

Step iv. Press >RESET BOARD<.

Step v. Press >SAVE TEST RESULTS<. A window will be displayed allowing a test file (.btr) to be created. Save results at regular intervals during the testing sequences so data will not accidentally be lost. This step automatically creates a board test report file (.btr) name based on the board serial number.

Step vi. A window, Clear Test Form Data?, will open. Select >NO< to preserve all test results.

Press the **Stage 3** button at the top of the Testing Panel window.
Stage 3. Mechanical Fit, Power Consumption and Firmware Programming Tests

Step i. Enter the firmware file names and Checksum/User codes according to the information noted during FPD Programming. See Appendix I.

Step ii. Use a digital Voltmeter to measure the power supply voltages at designated test points. See Figure 16 in Appendix I for test point locations.

Enter Current readings from Power Supply display for each voltage. Press the Output buttons 1 and 2 on the Power Supplies to toggle through the different voltages and current readings of each supply.

Step iii. Use a digital voltmeter to measure the reference supply voltages at designated jumper pins. See Figures 3 and 3A for jumper locations.

Step iv. Indicate jumper positions in spaces provided.

Step v. Compare the power consumption with that noted in Table 5 in Appendix II. LED D5 (Figure 13) on the component side of the Clock and Bias Board should be illuminated.

Using the Attribute Categories window, verify the board FPGA code ID in the Clock and Bias and Master Control boards. To do this select the CNB_Control page and press Update.

Verify clkCodeID. Press >UPDATE< Compare the displayed values to expected ones.

The first two numbers of the clkCodeID and the Firmware Version numbers of 18V02 EEPROM must match.

Step vi. Press >SAVE TEST RESULTS<. Press >YES< to overwrite existing file. Then press >NO< preserve all test data.

Click the Stage 4 button at the top of the Testing Panel window.

Stage 4. Basic Bus Transactions and System Clock Tests

Step i. Press >UPDATE VALUES<. Values will automatically update. The board serial number, ID Firmware and Board Temperature are dependent on the particular board under test. See Table 3 for a list of values and tolerances.
### Table 3 – Typical Telemetry Values

<table>
<thead>
<tr>
<th>Function</th>
<th>Value</th>
<th>Tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>VAB +Telemetry</td>
<td>+15V</td>
<td>±100mV</td>
</tr>
<tr>
<td>VAB – Telemetry</td>
<td>-15V</td>
<td>±100mV</td>
</tr>
<tr>
<td>VAC + Telemetry</td>
<td>+15V</td>
<td>±100mV</td>
</tr>
<tr>
<td>VAC – Telemetry</td>
<td>-15V</td>
<td>±100mV</td>
</tr>
<tr>
<td>+15VA Sup Telemetry</td>
<td>+15V</td>
<td>±100mV</td>
</tr>
<tr>
<td>-15VA Sup Telemetry</td>
<td>-15V</td>
<td>±100mV</td>
</tr>
<tr>
<td>+5VA Sup Telemetry</td>
<td>+5V</td>
<td>±100mV</td>
</tr>
<tr>
<td>-5VA Sup Telemetry</td>
<td>-5V</td>
<td>±100mV</td>
</tr>
<tr>
<td>Clk DAC Ref Telemetry</td>
<td>+2.49V</td>
<td>±10mV</td>
</tr>
<tr>
<td>Clk Channel 00-11 Offset Ref Telemetry</td>
<td>+2.49V</td>
<td>±10mV</td>
</tr>
<tr>
<td>Clk Channel 12-23 Offset Ref Telemetry</td>
<td>+2.49V</td>
<td>±10mV</td>
</tr>
<tr>
<td>Clk Channel 24-31 Offset Ref Telemetry</td>
<td>+2.49V</td>
<td>±10mV</td>
</tr>
<tr>
<td>Bias DAC Ref Telemetry</td>
<td>+2.49V</td>
<td>±10mV</td>
</tr>
<tr>
<td>Bias Channel 00-17 Offset Ref Telemetry</td>
<td>+2.04V</td>
<td>±10mV</td>
</tr>
<tr>
<td>Bias Channel 18-35 Offset Ref Telemetry</td>
<td>+2.04V</td>
<td>±10mV</td>
</tr>
<tr>
<td>Fast Bias DAC Ref Telemetry</td>
<td>0.0V</td>
<td>±10mV</td>
</tr>
</tbody>
</table>

**NOTE:** Power dissipation is calculated using the data obtained in Step 3ii.

Step ii. Press **TOGGLE D5 LED**. Observe D5 LED and ensure that it toggles on, then off. This indicates a successful link to the CBB. See Figure 13.

![D5 LED](image-url)

**Figure 13**
Step iii. Press **SAVE TEST RESULTS**. Press **YES** to overwrite existing file. Then press **NO** to preserve all test data.

Press the **Stage 5** button at the top of the Testing Panel window.

**Stage 5. Bias Voltage Functional Tests**

For this test sequence, verify the rainbow ribbon cable is connected to “Bias’s” on the breakout box. See Figure 4.

Step i. Press **SET BIAS DACS 10%**. Values will fill in automatically.

Step ii. Press **READ VOLTAGE TELEMETRY**. Values will fill in automatically.

Step iii. Press **READ CURRENT TELEMETRY**. Values will fill in automatically.

**NOTE:** Current Telemetry is a feature dependent of the specific board configuration. Thus, Current Telemetry values may or may not produce acceptable results. Verify specific board configuration to determine acceptability of Current Telemetry readings.

Step iv. Press **SET BIAS DACS 50%**. Values will fill in automatically.

Step v. Press **READ VOLTAGE TELEMETRY**. Values will fill in automatically.

Step vi. Press **READ CURRENT TELEMETRY**. Values will fill in automatically.

See **NOTE** in Step iii.

Step vii. Press **SET BIAS DACS 90%**. Values will fill in automatically.

Step viii. Press **READ VOLTAGE TELEMETRY**. Values will fill in automatically.

Step ix. Press **READ CURRENT TELEMETRY**. Values will fill in automatically.

See **NOTE** in Step iii.

Step x. Press **CALC DAC GRP MEANS**. Data will be displayed automatically.

Step xi. Press **CALC DAC SLOPES**. Data will be displayed automatically.

Step xii. Press **CALC TEL GRP MEANS**. Data will be displayed automatically.

Step xiii. Press **CALC TEL SLOPES**. Data will be displayed automatically.

Step xiv. Press **CALC TEL GRP MEANS**. Data will be displayed automatically.

Step xv. Press **CALC TEL SLOPES**. Data will be displayed automatically.

Step xvi. Press **DAC ISOLATION TEST**. The test will run automatically. The button changes to **WATCH FOR ANOMALIES** as the test runs.

Step xvii. Press **START BIAS NOISE TEST**. Values will fill in automatically.

Step xviii. Press **START BIAS RISE TIME TEST**. Observe the rise and fall times on the oscilloscope for BIASOUT0. Record rise time. Continue test by measuring and recording rise times for BIASOUT1 through BIASOUT35.
Step xix. Press >STOP BIAS TOGGLE<. Then press >SAVE TEST RESULTS<. Press >YES< to overwrite existing file. Then press >NO< to preserve all test data.

Press the **Stage 6** button at the top of the Testing Panel window.

### Stage 6. Fast Bias Functional Tests

For this test sequence connect the rainbow ribbon cable to “**Fast Biases**” on the breakout box. See Figure 4.

- **Step i.** Press >SET FAST BIAS DACS 10%<. Values will fill in automatically.
- **Step ii.** Press >READ TELEMETRY<. Values will fill in automatically.
- **Step iii.** Press >SET FAST BIAS DACS 50%<. Values will fill in automatically.
- **Step iv.** Press >READ TELEMETRY<. Values will fill in automatically.
- **Step v.** Press >SET FAST BIAS DACS 90%<. Values will fill in automatically.
- **Step vi.** Press >READ TELEMETRY<. Values will fill in automatically.
- **Step vii.** Press >CALC DAC SLOPES<. Data will be displayed automatically.
- **Step viii.** Press >CALC TEL SLOPES<. Data will be displayed automatically.
- **Step ix.** Press >DAC ISOLATION TEST<. The test will run automatically. The button changes to >WATCH FOR ANOMALIES< as the test runs.
- **Step x.** Press >START FAST BIAS NOISE TEST<. Values will fill in automatically.

Verify the green oscilloscope lead is connected to the GND bus pins on the breakout box. Connect the other measuring lead to the FBIAS0 pin of the P4 Fast Bias Outputs bank of the breakout box.

- **Step xi.** Press >START FAST BIAS TOGGLE<. Observe the rise and fall times on the oscilloscope for FBIAS0. Record rise times. Continue test by measuring and recording rise times for FBIAS1 through FBIAS7.
- **Step xii.** Press >STOP FAST BIAS TOGGLE<. Then press >SAVE TEST RESULTS<. Press >YES< to overwrite existing file. Then press >NO< to preserve all test data.

Press the **Stage 7** button at the top of the Testing Panel window.

### Stage 7. Clock Low DAC Functional Tests

For this test sequence, connect the rainbow ribbon cable to “**Clocks**” on the breakout box. See Figure 4.

- **Step i.** Press >SET LOW CLOCK DACS 10%<. Values will fill in automatically.
- **Step ii.** Press >READ TELEMETRY<. Values will fill in automatically.
- **Step iii.** Press >SET LOW CLOCK DACS 50%<. Values will fill in automatically.
Step iv. Press **Read Telemetry**. Values will fill in automatically.

Step v. Press **Set Low Clock DACs 90%**. Values will fill in automatically.

Step vi. Press **Read Telemetry**. Values will fill in automatically.

Step vii. Press **Calc DAC Grp Means**. Data will be displayed automatically.

Step viii. Press **Calc DAC Slopes**. Data will be displayed automatically.

Step ix. Press **Calc Tel Grp Means**. Data will be displayed automatically.

Step x. Press **Calc Tel Slopes**. Data will be displayed automatically.

Step xi. Press **Calc DAC ISOLATION TEST**. The test will run automatically. The button changes to **Watch for Anomalies** as the test runs.

Step xii. Press **Start Noise Test**. The test will run automatically.

Step xiii. Press **Save Test Results**. Press **Yes** to overwrite existing file. Then press **No** to preserve all test data.

Press the Stage 8 button at the top of the Testing Panel window.

**Stage 8. Clock Hi DAC and Dynamic Functional Tests**

Step i. Press **Set Hi CLK DACs 10%**. Values will fill in automatically.

Step ii. Press **Set Hi CLK DACs 50%**. Values will fill in automatically.

Step iii. Press **Set Hi CLK DACs 90%**. Values will fill in automatically.

Step iv. Press **Calc DAC Grp Means**. Data will be displayed automatically.

Step v. Press **Calc DAC Slopes**. Data will be displayed automatically.

Step vi. Press **Start Clock High DAC ISOLATION TEST**. Watch for anomalies. The button changes to **Watch for Anomalies** as the test runs.

Step vii. Press **Start Noise Test**. Values will fill in automatically.

Verify the green oscilloscope lead is connected to the GND bus pins on the Breakout Box. Connect the other measuring lead to the CLKOUT0 pin of the P2 Clock Outputs bank of the Breakout Box.

Step viii. Press **Start RiseTime Test**. Observe the rise and fall times on the oscilloscope for CLKOUT0. Record rise time.

Step ix. Continue test by measuring and recording rise times for CLKOUT1 through CLKOUT31.

Step x. Press **Stop Clock**. Then press **Save Test Results**. Press **Yes** to overwrite existing file. Then press **No** to preserve all test data.
Final Steps

1. At this stage the board can be considered fully functional.

2. Close the Board Testing Panel.
   Press >YES< to save Board Test, then Press >YES< to overwrite file.
   Press >SHUTDOWN PAN< on the MEC. Then close any remaining windows on the screen.
   Shut down the Power Supplies in the reverse order in which they were turned on.
   Shut down the Data Acquisition Unit and the oscilloscope.

3. Update the ART file and ensure that the filename for the test report correctly reflects the product code and serial number of the board and store it in the directory:
   \big-boy\MonsoonAdmin\Production\TST_Repository\TestResults\ClkBiasBrdRev_1

4. Make an Acrobat .pdf copy of the same file and store it in the directory:
   \big-boy\MonsoonAdmin\Production\HIST_Repository\ClkBiasBrdRev_1\SNxxx

5. Follow the steps in Appendix III to create an HTML file for the newly created test report.
2.0 Appendix I - JTAG Usage and Field Programmable Device (FPD) Setup

2.1 Appendix I Clock and Bias Board FPD Programming

To start the iMPACT tool, double-click on the icon on the desktop. A series of windows opens asking the operator for a selection. They are:

- Boundary-Scan Mode. Select >AUTO CONNECT…<. Press >FINISH<.

Step i. With the iMPACT JTAG tool initialized, confirm that four devices are seen as follows. See Figure 14:

- FPGA EEPROM store (U200 –xc18v02)
- FPGA itself (U116 – xcv300e)
- CPLD (U119 – xcr3384xl)
- CPLD (U118 – xcr3384xl)

![iMPACT Tool Window with JTAG Chain](image)
Step ii. Press >CANCEL ALL< in the Assign New Configuration File window.

Step iii. Using Windows Explorer, locate the following file folder:

Mnsn on ‘bigboy’/MonsoonAdmin/Production/TST_Repository/TestProcedures/Firmware

The above folder contains the latest configuration firmware revision document.

The document name is:

**Existing Firmware Products for Monsoon xxxxxxxx.doc**

where xxxx is the last revision date.

Open the latest firmware revision document and find the Clock and Bias section. The latest information will be designated with a green shaded area. **Use this document as a reference to verify all latest Firmware Versions.**

Step iv. To program the devices, begin by right clicking on the first device. A drop down menu appears. Select >ASSIGN NEW CONFIGURATION FILE<. See Figure 15.

![iMPACT Tool Window with Menu](image)

Figure 15
Step v. Follow the previous path on *big boy* to the *Firmware* folder, then open the latest *ClkBiasFpgaVxx folder* and select the latest *ClkBiasFpgaVxx.mcs* file. Click on *OPEN* and the file will be assigned to the selected device. Make a note of the loaded Firmware filename, as it will be entered later into the Testing Panel.

Step vi. The second device will not be programmed. Right-click on the second device. A drop down menu appears. Select *BYPASS*.

Step vii. For the third device open the latest *ClkBiasCfgCpldVxx* folder and select the latest *ClkBiasCfgCpldVxx.jed* file. Click on *OPEN* and the file will be assigned to the selected device. Make a note of the loaded Firmware filename, as it will be entered later into the Testing Panel.

Step viii. For the fourth device open the latest *ClkBiasSeqCpldVxxx* folder and select the latest file named *ClkBiasSeqCpldVxxx.jed*. Again, click *OPEN* and the file will be assigned to the selected device. Make a note of the loaded Firmware filename, as it will be entered later into the Testing Panel.

Step ix. Cycle power to the chassis by shutting down the power supplies in the reverse order in which they were turned off, then turn them on again in sequential order (Refer to step ii of Stage 3).

Step x. In the iMPACT tool window pull down the ‘File’ menu and select *INITIALIZE CHAIN*, Then select *CANCEL ALL*.

With the iMPACT JTAG tool, verify that the proper code is present in both FPGAs, which should now have booted its own code from the EEPROM. The CBB Status light should be illuminated at this point. See Table 4.

Step xi. Right click on the first, third and fourth devices in turn and select *GET DEVICE CHECKSUM* from the drop-down menu.

**NOTE:** The checksum results will appear in the light blue area of the iMPACT window.

Do this for the first, third and fourth devices. Make sure the checksum data matches that in the 

*Existing Firmware Products for Monsoon xxxxxxxx.doc* file.

Make a note of the checksum result. It will be entered later into the Testing Panel.

Step xii. For the xcv300 device right click on the device icon and select *GET DEVICE SIGNATURE/USER CODE*. Verify that the user code matches that in the *Existing Firmware Products for Monsoon xxxxxxxx.doc* file.

Make a note of the user code result, as it will be entered later into the Testing Panel.
Step xiii. Exit the iMPACT tool. Do not save changes.

Close the Existing Firmware Products for Monsoon xxxxxxxxx.doc.

Shut down the power supplies in the reverse order in which they were turned on.

Disconnect the JTAG Programming Cable from the CBB.

Return to Stage 3, Step iv of the testing sequence.

Table 4 - JTAG Device Description

<table>
<thead>
<tr>
<th>JTAG Order</th>
<th>Designator</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>U200</td>
<td>18V02 EEPROM FPGA configuration store</td>
</tr>
<tr>
<td>2</td>
<td>U116</td>
<td>Virtex300E FPGA Buss Interface</td>
</tr>
<tr>
<td>3</td>
<td>U119</td>
<td>Coolrunner XCR3384 Configuration CPLD</td>
</tr>
<tr>
<td>4</td>
<td>U118</td>
<td>Coolrunner XCR3384 Sequencer CPLD</td>
</tr>
</tbody>
</table>

Test Point Locations

Figure 16
2.2 Appendix II. Power Consumption Tables

These tables outline the power consumption for a correctly operating board alone in a MONSOON chassis under test conditions:

2.2.1 Before Programming Power Consumption Tables

Table 5 - Power Supply Requirements (before programming)

<table>
<thead>
<tr>
<th>Supply Name</th>
<th>Set Voltage</th>
<th>Nominal Current with Internal 3.3v Generation</th>
<th>Nominal Current with External 3.3v Supply</th>
<th>Overcurrent Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3VD</td>
<td>3.3v +/- 50mv</td>
<td>0.00 amps</td>
<td>0.180 amps</td>
<td>1.0 amps</td>
</tr>
<tr>
<td>5VD</td>
<td>5.0v +/- 100mv</td>
<td>0.25 amps</td>
<td>0.15 amps</td>
<td>1.0 amps</td>
</tr>
<tr>
<td>+5VA</td>
<td>+5v +/- 100mv</td>
<td>0.35 amps</td>
<td>0.35 amps</td>
<td>1.0 amps</td>
</tr>
<tr>
<td>-5VA</td>
<td>-5v +/- 100mv</td>
<td>0.01 amps</td>
<td>0.01 amps</td>
<td>0.5 amps</td>
</tr>
<tr>
<td>+15VA</td>
<td>+15v +/- 100mv</td>
<td>0.20 amps</td>
<td>0.20 amps</td>
<td>1.0 amps</td>
</tr>
<tr>
<td>-15VA</td>
<td>-15v +/- 100mv</td>
<td>0.30 amps</td>
<td>0.10 amps</td>
<td>1.0 amps</td>
</tr>
</tbody>
</table>

NOTE: Depending on the time constant set in the bias voltage amplifier, it may be necessary to wait several seconds for the voltage levels to settle before measuring the voltage of the signal.
2.2.2 After Programming Power Consumption Tables

Table 6 - Power Supply Requirements (after programming)

<table>
<thead>
<tr>
<th>Supply Name</th>
<th>Set Voltage</th>
<th>Nominal Current with Internal 3.3v Generation</th>
<th>Nominal Current with External 3.3v Supply</th>
<th>Overcurrent Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3VD</td>
<td>3.3v +/- 50mv</td>
<td>0.00 amps</td>
<td>1.80 amps</td>
<td>1.0 amps</td>
</tr>
<tr>
<td>5VD</td>
<td>5.0v +/- 100mv</td>
<td>0.25 amps</td>
<td>0.15 amps</td>
<td>1.0 amps</td>
</tr>
<tr>
<td>+5VA</td>
<td>+5v +/- 100mv</td>
<td>0.35 amps</td>
<td>0.35 amps</td>
<td>1.0 amps</td>
</tr>
<tr>
<td>-5VA</td>
<td>-5v +/- 100mv</td>
<td>0.01 amps</td>
<td>0.01 amps</td>
<td>0.5 amps</td>
</tr>
<tr>
<td>+15VA</td>
<td>+15v +/- 100mv</td>
<td>0.20 amps</td>
<td>0.20 amps</td>
<td>1.0 amps</td>
</tr>
<tr>
<td>-15VA</td>
<td>-15v +/- 100mv</td>
<td>0.30 amps</td>
<td>0.10 amps</td>
<td>1.0 amps</td>
</tr>
</tbody>
</table>

Table 7 - Overcurrent Protection Settings for MCB plus Clock and Bias Boards

<table>
<thead>
<tr>
<th>Supply Name</th>
<th>Nominal Current with Internal 3.3v Generation</th>
<th>Nominal Current with External 3.3v Supply</th>
<th>Overcurrent Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3VD</td>
<td>0.90 amps</td>
<td>1.00 amps</td>
<td>2.5 amps</td>
</tr>
<tr>
<td>5VD</td>
<td>0.60 amps</td>
<td>0.50 amps</td>
<td>1.5 amps</td>
</tr>
<tr>
<td>+5VA</td>
<td>0.35 amps</td>
<td>0.35 amps</td>
<td>1.0 amps</td>
</tr>
<tr>
<td>-5VA</td>
<td>0.01 amps</td>
<td>0.01 amps</td>
<td>0.5 amps</td>
</tr>
<tr>
<td>+15VA</td>
<td>0.20 amps</td>
<td>0.20 amps</td>
<td>1.0 amps</td>
</tr>
<tr>
<td>-15VA</td>
<td>0.30 amps</td>
<td>0.30 amps</td>
<td>1.0 amps</td>
</tr>
</tbody>
</table>
2.3 Appendix III Creating an HTML Test Report

The following steps describe how to create a readily usable HTML file from the .btr file created by the Test Platform.

Step i. Open an xterm window and locate the following directory:

/home/monsoon/BoardTests

Step ii. Verify the *clkBrdTestReport.tcl* file is in the BoardTests directory

Step iii. On the xterm command prompt type the following command:

```
wish clkBrdTestReport.tcl
```

Step iv. A window will open requesting that a .btr file be selected and saved.

- Open the desired CBB serial number folder and then open the desired .btr report to be printed.
- Save the selected file in the same location as the .btr file being selected.

Step v. Exit the xterm window

The new .html version of the test report can now be opened and printed through any web browser.