REASON FOR MODIFICATION:
Compatibility issues with PECL clocks generated by the LMK03000 device. CLK3, CLK4, CLK5 are PECL outputs on the LMK03000. These need to be level converted to feed the FPGA clock inputs. Placement of required termination resistor on the differential inputs of the SCAN90CP02 device.

DRAWINGS AFFECTED:
TRNT-EL-04-2001 r1.6 1.7

DESCRIPTION OF MODIFICATION:

1. Close to the LMK03000 device insert six series resistors of 70 Ohms into each differential signal on from pins 23, 24, 38, 39, 41, and 42 of U2. Signals are TCLK+/-, MCLK+/-, PCLK+/-.

2. After these resistors and still close to the LMK03000 device insert three shunt resistors across the differential pairs of value 187 Ohms.

3. Add two shunt resistors of 100 Ohms in close proximity to the differential signal inputs of U4 between pins 9 and 10, and between pins 13 and 14.