NOAO
ENGINEERING CHANGE ORDER

BOARD NAME TORRENT Local Control Board (LCB)  ECO# TRNT-012  DATE 9/15/2010
BRD SERL# Starting at 005  REV   ART#
PN# REV OD  REV OD
ASBLY# TRNT-EL-04-0002  REV OD  PCB# TRNT-EL-04-1002  REV OD
BOM# TRNT-EL-04-4002  REV OD  SCH# TRNT-EL-04-2002  REV OD
COGNIZANT ENGNR APPROVD

REASON FOR MODIFICATION:
Functional corrections to physical and electrictric elements

DESCRIPTION OF MODIFICATION:

<table>
<thead>
<tr>
<th>Item</th>
<th>Originator</th>
<th>Action Description</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 dms</td>
<td>fix item #74 on bom to correct PN 16 term CTS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 dms</td>
<td>replace vias with direct connect vias - at least correct thermals</td>
<td></td>
<td></td>
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<tr>
<td>3 dms</td>
<td>bga and lga parts all vias under should be barrel relieved. fix L10 on layout to correct component outline</td>
<td></td>
<td></td>
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<tr>
<td>4 dms</td>
<td>please provide complete PN</td>
<td></td>
<td></td>
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<tr>
<td>5 dms</td>
<td>add a ground strap to the board and/or loop test points replace U31, with new library element to reflect correct size</td>
<td></td>
<td></td>
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<tr>
<td>6 dms</td>
<td>of part, move R52 away from the U31</td>
<td></td>
<td></td>
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<tr>
<td>7 dms</td>
<td>make sure gerber pad data is solid pads look at reducing the pad size on all NLSX3014 parts to allow some mask between lands. Make resist tight on sides of pad but leave room for fillets on the ends.</td>
<td></td>
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<tr>
<td>8 dms</td>
<td>review camtek email on 3/30/09 (7) issues with gerber</td>
<td></td>
<td></td>
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<tr>
<td>9 dms</td>
<td>PL #23 add C239 in refdes column</td>
<td>complete</td>
<td></td>
</tr>
<tr>
<td>11 dms</td>
<td>shield connection on J8, J9, j10</td>
<td></td>
<td></td>
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<tr>
<td>12 dms</td>
<td>Fiducial near U37 clear top layer copper pour away more</td>
<td>complete</td>
<td></td>
</tr>
<tr>
<td>13 dms</td>
<td>C148 move &quot;+&quot; to better location</td>
<td>complete</td>
<td></td>
</tr>
<tr>
<td>14 dms</td>
<td>J4 needs pin 1 marking on SS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15 dms</td>
<td>U80 pin 1 marking move off via</td>
<td>complete</td>
<td></td>
</tr>
<tr>
<td>16 dms</td>
<td>c117 skewed part fix thermal imbalance</td>
<td>complete</td>
<td></td>
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DRAWINGS AFFECTED:
NEW
REV
TRNT-EL-04-0002 A
TRNT-EL-04-1002 A
TRNT-EL-04-2002 A
TRNT-EL-04-3002 A
TRNT-EL-04-4002 A

M:\engr_Development\Torrent\DOC_CTRL\ECOs\ECO_Released\TRNT-012\TRNT-012.doc
Part list add 2 rohs labels, note on assembly locations

20 dms R13 line it up components above it

21 dms selection of I2C serial number part

add I2C serial number IC & connections (addressing issue)

LCB EEpom U25 4 (1,2,7 = gnd)(3 = 3.3V) fix
LCB TS1 U26 1 (5,6 = gnd)(7 = 3.3V) okay
LCB TS2 U57 2 (5,6, 7 = gnd) okay

22 dms LCB SSN N/A N/A N/A N/A need to

Change SPT connector for fixed transceiver - if the GiGe product wors. This would prevent accidental extraction of transceiver when trying to remove fibers.

PCM

replace lib element LTM4608 (U37&U20) in schematic, this should disconnect 4C & 5C from the SVIN net. Remove traces from 4C & 5C

24 dms change fan connector to right angle and move toward tab so that it will fit.

25 dms swap sides of board reset sw & fan con

26 pcm review lt3080 package options to MS or DD

27 pcm P4, add pins for digital ground.

29 dgs/pcm Reverse connections to FPGA pins G1 and H1. G1 should be SPF_RD+ and H1 should be SPF_RD-.

Add a low pass filter to pin 32 (CP) of LMK03000 clock conditioner. I've worked out some values for the three components that we need to put on the CP node (pin 32) of the LMK03000 device (U28) on the LCB board. Please update the redline for the LCB and if possible, try to kludge these on the LCB prototype board in Tucson for test.

1. From pin 32 on U28 connect a ceramic 5% 5.6nf 25v NPO capacitor to ground.

2. From pin 32 on U28 connect a ceramic 5% 7.5nf 25v NPO capacitor via a 1% 3.60K series resistor to ground.

31 pcm Seriously look at supplying a separate and localized 2.5v supply to the GiGe device close to the flex connector. As it is the supply to the GiGe is @ 2.42volts due to the voltage drop across the pcb lands from U9. In addition, this would better isolate the GiGe digital noise from the LCB logic.

32 pcm Remove R66 and connect u27 PIN n22 (/CS_B_0) to gnd

33 pcm Consider replacing the SFP modular Fiberxon FTM-8120C-LG transceiver with a board mount version Intel TXN310110000000

34 all silk screen slot label "AFE1* & "AFE2" by the correct connectors rename all "AFE1_..." to "AFE2_..." and "AFE0_..." to "AFE1_..." before editing net names send off a was/is list for approval. In the I2C area

35 pcm 1. Remove signal I2C_SNS_EN from U22 pin 12. Connect pin 12 U22 to pin 1 U22 (VL):
2. Remove signal I2C_SRC_EN from U23 pin 4. Connect the signal I2C_SNS_EN from step one to U23 pin 4. Rename the signal I2C_SNS_EN as I2C_SDA_EN.

3. Swap signals from the inputs and outputs of U23 pin 2 (input) and 7 (output) with U24 pin 2 and 7.

4. Remove signal I2C_SRC_EN from U66 pin 12. Connect pin 12 U66 to pin 1 U66 (VL) +2.5V.


6. Swap signals from the inputs and outputs of U67 pin 2 (input) and 7 (output) with U14 pin 2 and 7.

7. Rename the signal I2C_SRC_EN to be I2C_SCL_EN.

1. Disconnect signal LCB_RESET from pin 9 (/1A) of U70 leaving the pullup (R18) connected to the FET drain (Q3).

2. Disconnect signal /REBOOT from pin 11 (/R) of U70 and reconnect to pin 9 (/1A) of U70 leaving the resistor and capacitor (R105 & C231) connected to pin 11.

4. Add shunt 180 Ohm resistors on the above nets to GND.

3. Change the value of the termination resistors R31, R37, R82 to be 100 Ohms.

4. Add shunt resistors and termination resistors to clock net DCLK.

TSM_PRESENT, ~TSM_PRESENT (J13) what is the permanent solution

R24 - move to bottom of the board so that part will solder to the board.

Correction OCLK PECL Termination: (following 2 items)

1. Add a 180 Ohm shunt resistor from FPGA pins J14, H13 (OCLK, /OCLK) to GND

2. Add a 100 Ohm termination resistor between these signals and as close as possible to the FPGA pins.

1. Remove GND connection from the memory device U31:A balls F3 and B3

2. Connect U31:A ball F3 to signal LDM (ball V25 on FPGA - U27:F)

3. Connect U31:A ball B3 to signal UDM (ball W29 on FPGA - U27:F)

move J4 up about .2 inches and add a 9th pin that goes to ground.

LS2 connector, graphic depicting orientation of socket /pin in silkscreen
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<tr>
<td>dms</td>
<td>make sure all LFN, DFN package parts have enough pad</td>
<td>(LTC2801CDE#PBF &amp; NLSX3014MUTAG)</td>
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<tr>
<td>59</td>
<td>6/09/10</td>
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