REASON FOR MODIFICATION:
1. Prevent power supplies VANA, VCB, VHV, VBB from turning on during initial FPGA configure at power on. This causes potential lethal voltages (for detectors) to appear on the detector output pins.

DESCRIPTION OF MODIFICATION:
1. Place diodes on U8:2 VCB_PWR_EN_OUT, U8:11 VANA_PWR_EN_OUT, and U8:15 VBB_ENBL_OUT.
   - with anodes to U8 pins - and common cathodes tied together and connected to the DONE signal that can be found R64:2, TP5, U27:M15 & U43:13. See graphics for installation locations.

On bottom of board (opposite the Xilinx BGA)
See Figure 1 and 2, Figure 3 and 4 are additional information
Solder D2:2 to via highlighted in red, Solder D3:1 to via highlighted in red
Use white 30 or 32 awg wire, solder one end to red via by R107, the other end to lead of D2 (D2:1)
Use white 30 or 32 awg wire, connect D3:3 (K) to D2:3, connect D2:3 to TP5. Use RTV to tack long wire approximately where shown by the green X marks, avoid all pads & vias.
2. The following resistors are normally not installed: R68, R69, R108, R109

This section to be completed by reviewing authority

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Disposition:  □ Approved  □ Denied  □ Request Additional Information
2. Remove resistors R68, R69, R108, R109

- R68 - Enables the use of the 'boot after eeprom write' function of the JTAG interface
- R69 Selects the clkout phase of U37
- R108, R109 when installed, selects the backup firmware load on the GIGe interface