REFERENCE: WISHBONE BUS INTERCONNECTION SCHEME
See http://www.opencores.org/projects.cgi/web/wishbone/wishbone

WISHBONE USER-DEFINED SIGNAL DEFINITIONS

<table>
<thead>
<tr>
<th>TGD_3D Code</th>
<th>Significance</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Normal Read/Write Bus Cycle</td>
</tr>
<tr>
<td>1</td>
<td>Broadcast Bus Cycle (Always Space)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TGD_3D Code</th>
<th>Significance</th>
</tr>
</thead>
<tbody>
<tr>
<td>0'</td>
<td>Normal Bus Cycle</td>
</tr>
<tr>
<td>1'</td>
<td>Normal Bus Cycle</td>
</tr>
<tr>
<td>10'</td>
<td>16-Bit Wide Bus Cycle</td>
</tr>
<tr>
<td>11'</td>
<td>32-Bit Wide Bus Cycle</td>
</tr>
</tbody>
</table>

WISHBONE 'USER DEFINED' SIGNAL DEFINITIONS

CHANGES FROM VERSION C1 TO C2
1. Moved Sequencer logic from LCB control module to CFG Services module.

Significance
- Normal Read / Write Bus Cycle
- Broadcast Bus Cycle (Machine State)

TGD_I/O Code | Significance
-------------|--------------|
'0'          | Reset Bus Cycle  |
'0'          | Read Bus Cycle  |
'1'          | 16-Bit Write Bus Cycle |
'1'          | 32-Bit Write Bus Cycle |

TGD_I/O Code | Significance
-------------|--------------|
'00'         | TGC_I/O Code  |
'01'         | '01'         |
'10'         | '10'         |
'11'         | '11'         |

CHANGES FROM VERSION C2 TO C3
1. Corrected signal arrow on page 7 to point to page 2 rather than page 3.
2. Removed multiplexor from page 3.
3. Renumbered pages.
4. Colored blocks orange to indicate available firmware from MONSOON Orange.
5. Added extra level of hierarchy to I2C_Sequencer logic on page 3.
MONSOON TORRENT
LCB FIRMWARE ARCHITECTURE

NAME

DWG NO

RELEASED

SIZE REF REV

PAGE OF

StreamDataRdy

StreamData

StreamDataAddress

StreamDataClk

PAGE 5

6 x 8

C3

NATIONAL OPTICAL ASTRONOMY OBSERVATOIES

C

PAGE 6

C

PING-PONG FIFO MATCHES THE

PIXEL DATA RATE TO THE IMAGE

BUFFER MEMORY BURST SIZE

2 x 18 x 8

DEEP

FIFO

ACQ

CONTROL

WrtFifo

RdFifo

Chan2DataOut

FifoRdSlct

Chan2FifoRdReq

Chan2FifoRdAck

Chan3DataOut

TCLK

Chan0DataOut

Chan1DataOut

Chan4DataOut

Chan5DataOut

Chan6DataOut

ADC BUSY DETECTION

SYNTHETIC PIXEL GENERATOR

SerialDataGate

ChanSynthDataType

AFE_DATA[0]

AFE_DATA[1]

AFE_DATA[2]

AFE_DATA[3]

AFE_DATA[18]

AFE_DATA[19]

AFE_DATA[20]

AFE_DATA[21]

ADC CLOCK GENERATOR

TCLK

CTC DETECTOR

/8

/1

/1

SynthDataGate

CtcDetect

ADC BUS ARBITRATION LOGIC -

FROM PAGE ??

AFE_CDS[0:7]

AFE_CDS_STB[1]

AFE_CDS_STB[0]

AdcAcqDataRequest

AdcAcqDataEnable

TO PAGE 7

AFE1_ADC_STB

AFE_PWRDATA[60]

AFE_PWRDATA[62]

AFE_PWRDATA[0]

AFE_PWRDATA[1]

AFE_PWRDATA[2]

AFE_PWRDATA[3]

AFE_PWRDATA[18]

AFE_PWRDATA[19]

AFE_PWRDATA[20]

AFE_PWRDATA[21]

CCD AFE INTERFACE SIGNALS