Bus interface and digital control

From CLOCKs

From BIASes

From CLOCKs

From CCD ADCs

From BIASes

To CCD ADCs

Pg. 7 & 8

Spare output from AFE to LCB

Clock DAC Voltage Telemetry

AFE Offset DAC Voltage Telemetry

Analog Section Control Signals

Notes:

CTC_OUT     <= not CDS_latch(0);
INVERT_SIG  <= not CDS_latch(1);
NONINV_SIG  <= not CDS_latch(2);
INTEGRATE   <= not CDS_latch(3);
DC_RESTORE  <= not CDS_latch(4);
RESET_INT   <= not CDS_latch(5);
Need to calculate a Pi circuit for 1MHz

Main Power

Digital Power

Incoming Supply filtering

Interface Power

Need to limit this to ±6V max

NOTE: ± VANA minimum now 10.5V

-3.3V / -32.2V

Keep isolated from the other power

+31.6V / +2.7V

NOTE: + - VANA minimum now 10.5V

Digital Power

Clocks & Biases Power Supplies & References

Analog low noise Signal Chain Power Supplies and References

APPROVED FOR
REFERENCE
12/12/11 DMS
DAC0_VOUT0 -07 are for Biases

DAC0_VOUT8 - 11 are for HV Biases
Temp sensors should be positioned opposite sides (top/bottom) and ends (horizontal/vertical) from each other.

Isolation lines should be used on the ground plane under each channel to prevent return current crosstalk.

Pins 15, 18, 19 have separate ground pour on Layer 7, return for preamp +10V