TORRENT
AFE CCD
Test Procedure

NOAO Document TRNT-TS-01-0004
Revision: 0

Authored by:
Kathie Zelaya, Ron George
1/26/2012

Please send comments:
kzelaya@noao.edu

Created on 1/26/2012

Page 1 of 22
## Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date Approved</th>
<th>Sections Affected</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1/26/2012</td>
<td>All</td>
<td>Original Version</td>
</tr>
</tbody>
</table>

Created on 1/26/2012

Page 2 of 22
# Table of Contents

Revision History ................................................................................................................. 2
Table of Contents ............................................................................................................... 3
List of Figures ....................................................................................................................... 4
List of Tables ........................................................................................................................ 4

## 1.0 Introduction .................................................................................................. 5

### 1.1 Required Equipment ...................................................................................... 6

### 1.2 Test Schedule ................................................................................................... 6

- Stage 1 Preparation of Documentation ................................................................. 6
- Stage 2 AFE Board Test Setup ............................................................................. 8
- Stage 3 AFE Testing Sequence .............................................................................. 9
  - 3.1 AFE Initialization .......................................................................................... 9
  - 3.2 AFE Supplies ............................................................................................... 12
  - 3.3 AFE Control ............................................................................................... 12
  - 3.4 AFE Clocks ............................................................................................... 13
  - 3.5 AFE Bias .................................................................................................. 14
  - 3.6 AFE Video ............................................................................................... 17
- Stage 4 AFE Electronics Performance Analysis ....................................................... 19
  - 4.1 Image Data Retrieval ................................................................................. 19
  - 4.2 Preliminary Image Data Analysis ................................................................. 20
  - 4.3 Image Data Transfer .................................................................................. 21

## 2.0 Appendix ....................................................................................................... 22

### 2.1 AFE Channel Region Definitions ................................................................. 22

- Table 1. AFE Channel region Coordinates .......................................................... 22

### 2.2 Noise Figure Limits ...................................................................................... 22

- Table 2. Noise Figure Limits ............................................................................... 22
List of Figures

Figure 1. Typical AFE Board..........................................................................................7
Figure 2. Video Input Shorting Plug Installation ............................................................8
Figure 3. Torrent Input Ports..........................................................................................8
Figure 4. Fiber Link and Buffer Status.........................................................................9
Figure 5. mBORG Window Display ...........................................................................10
Figure 6. MEC Pan Windows......................................................................................11
Figure 7. AFE Supply Test Point Locations ............................................................12
Figure 8. AFE Clock Locations................................................................................13
Figure 9. Typical instat result display .......................................................................20

List of Tables

Table 1. AFE Channel region Coordinates................................................................22
Table 2. Noise Figure Limits ..................................................................................22
1.0 Introduction

This document covers the testing strategy for the TORRENT Analog Front End (AFE) to take the board from post-manufacture to a fully functional state. All tests described in this document pertain to the latest hardware revision level of the subject board. The tests described here do not prove that the board under test will meet specification but do test the full functionality of the board and identify failures that may be the result of component and manufacture problems. The test procedure assumes that the tester is familiar with the use of the mBORG Engineering Console (MEC) and can execute the required commands. The tests are divided into progressive stages ranging from 1 to N. Each higher number stage uses assumptions on the board condition that requires the previous stages to have been successfully completed.

In the description for these tests, certain conventions are followed to ease comprehension. These conventions and examples of each are presented in Table 1.

Table 1 - Test Description Conventions

<table>
<thead>
<tr>
<th>Convention</th>
<th>Example</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linux commands that are typed on a PAN xterm window</td>
<td>mecStart</td>
<td>Boldface italics</td>
</tr>
<tr>
<td>Values typed to the MEC</td>
<td>“noise1.ucd”</td>
<td>Character in quotes</td>
</tr>
<tr>
<td>Buttons on the Detector Head Electronics (DHE) boards or MEC console</td>
<td>&gt;startExp&lt;</td>
<td>Bold italics underlined inside &gt; &lt; symbols</td>
</tr>
<tr>
<td>Linux commands that are typed for iraf image analysis</td>
<td>dir</td>
<td>Italic</td>
</tr>
<tr>
<td>Specific board signal names</td>
<td></td>
<td>boldface small capitals</td>
</tr>
<tr>
<td>MEC attribute names</td>
<td>mcbCodeID</td>
<td>Boldface italics</td>
</tr>
</tbody>
</table>

The result of each test will be recorded on an Acceptance Test Report Checklist, TRNT_EL_08_xxxxSNnnnn (where SNnnnn is the serial number). This file should be saved to the official document control area of the TORRENT project in the following directory:

\big-boy\MNSN\engr_Development\Torrent\DOC_CTRL\EL-08\08-0004_AFE

This file shall be deemed the official record of the test results that may be printed out and kept in the system binder and/or supplied to the end user. All entries of data shall be made as required per this test Procedure and the Acceptance Test Report Checklist.
1.1 **Required Equipment**

- Torrent Test Unit
- 24V Brick Power Supply
- Fiber Cable connection to a working PAN
- Personal Computer running MS Windows 2000 or Windows XP. The PC must be connected to the network with the `\big-boy\MNSN` disk mapped into the Windows disk structure. Required programs are Word and WinaXe which allow connections to the mBORG software.

OR

Personal Computer running LINUX

- Oscilloscope - Agilent MSO7034B
- Digital Mutimeter –Fluke 77 or equivalent
- Video Input Shorting Plug (xxxxx)
- PSM Connector Grounding Plug (xxxxx)
- Grounding Cable (xxxxx)

1.2 **Test Schedule**

**Stage 1  Preparation of Documentation**

**Step 1.1.1** Locate the Assembly Record Tag (ART) for the AFE Board to be tested. The ART is a record of every action that has been taken on the board. AFE ARTs are located in:

`\big-boy\engr_Development\Torrent\DOC_CTRL\EL-07_ARTs\07-0004_AFE_CCD`

Locate testing info section and insert relevant test info as required
Step 1.1.2 Using a comparison photograph or a known good board, visually inspect the board for physical damage, missing and misplaced components. Figure 1 shows a typical AFE Board. The particular board under test may not have exactly the same layout as pictured.

![Typical AFE Board](image)

**Figure 1. Typical AFE Board**

Step 1.1.3 Note and correct any non-conformances. Save the ART record, as required.

Step 1.1.4 Locate the AFE Test Report Template. This template must be used to document the testing sequence and measured test values. This report shall be reviewed by the Project Engineer for acceptance of the overall board performance.

The AFE Test Report Template can be located in:

`\big-boy\engr_Development\Torrent\DOC_CTRL\EL-08\08-0004_AFE_CCD`
Stage 2 AFE Board Test Setup

Step i  Locate the Torrent Test Unit and remove the Top Cover (if required). Insert the AFE under test into the AFE1 slot of the Local Control Board (LCB). Secure the newly inserted AFE in the blue guide rails by using the white lock tabs on either side of each rail. Install the Video Input Shorting Plug into the J2 connector of the AFE under test.

![Video Input Shorting Plug](image1)

**Figure 2. Video Input Shorting Plug Installation**

Step ii  Locate the Test 24V Brick Power Supply and connect it to the Power Port on the Torrent Test Unit. See Figure 3.

![Torrent Input Ports](image2)

**Figure 3. Torrent Input Ports**

Created on 1/26/2012

Page 8 of 22
Step iii Locate the Power Supply Grounding Plug and cable. Complete installation by inserting into Test Unit connector port. See Figure 3.

Step iv Connect the Fiber Optic Cable into Test Unit fiber optic port. See Figure 3.

Stage 3 AFE Testing Sequence

3.1 AFE Initialization

Step 3.1.1 Turn on Test Unit by pressing and holding the Power Button for TWO seconds then release. Successful Test Unit power up is achieved by verifying that the: Green LED Power Button illuminates, fan blower turn on and Red LED status lights illuminate on the RS244 LCB Connectors. See Figure 2.

Step 3.1.2 Open one xterm window on the PAN. In the first xterm window, type fs0 and look at the fiber link status. The status will probably show data in the receive FIFO buffer and should show the DHE to be in reset mode by having the dir(ection) bit true in the IO register \(i=01xx0\). The status command should return something similar to the following:

```
FibreXtreme (SL) Monitor (sl_mon) rev. 3.02 (2003/10/06)  
Driver: rev. b2-835455:776764 for Linux with API rev. 2.1  
Hardware: unit/bus/slot 0/1/4 - SL100 (D64) Firm. 1C.13 (1C.13)  
for 5.0V PCI  
   Link Control Register (CSR 0x08) = 0x37  
   Link Status Register (CSR 0x0c) = 0x200 Link is UP  
   FPDP Flags Register (CSR 0x10) = 0x200 NR.D.P2.P1.S:  
      i=01110 o=00000  
   FIFO Threshold Register (CSR 0x14) = 0x0 Int.thr. = 0x0  
      Data count = 0xE75D (59229) bytes  
   Link (and other) Errors = 3  
Configurable parameters:  
   Loop Configuration:  0 (Point-to-Point)  
   Max Timeout:  600000 (6000000 ms)  
   Flow Control:  0 (NO) Halt on link error:  
      1 (YES)  
   CRC generate/check:  1 (YES) Allow Queuing on link error:  
```

Figure 4. Fiber Link and Buffer Status
Step 3.1.3 Use the command fc0 to clear the read buffer. Confirm with the status command that the read FIFO buffer is now empty (Data count = 0x0 (0) bytes) and that no link errors persist.

**NOTE:** Before proceeding, know that the mBORG Manual Test code can be found in the “mastodon” PAN network name. A directory in which to store the acquired data for test analysis must be created in the following location on “mastodon”:

/data/AFETests

Create and name the directory using the serial number of the AFE under test. For example, if AFE serial number 001 is being tested, the directory name must be:

sn001

Step 3.1.4 In the xterm window, start the PAN software and the mBORG using the command:

`runManual mastodon &`

The mBORG Engineering Console (MEC) and mBORG Welcome windows will be displayed as shown in Figure 3.

![mBORG Window Display](Figure 5. mBORG Window Display)
Step 3.1.5  Press the **>CONNECT<** button on the MEC. The four pan Windows will be displayed as shown in Figure 6.

![Figure 6. MEC Pan Windows](image)

Step 3.1.6  Press the **>DHE CONTROL<** button and execute a Reset DHE sequence by selecting “Reset DHE” from the pull down menu.

Step 3.1.7  Press the **>DHE CONTROL<** button again and execute an Initialize DHE sequence by selecting “Initialize DHE” from the pull down menu.
3.2 AFE Supplies

Step 3.2.1 In the MEC window, press the >ATTRIBUTES< button. Select the “AFE Supplies” option from the pull down menu. The AFE Supplies Attribute Display window will appear for reference to the vhv, vcb, and vana Voltages.

Step 3.2.2 Measure the AFE Supply voltages at their designated test points. Record the results on the Manual AFE Acceptance Test Checklist where provided. Refer to 7 for AFE Supply Test point locations.

3.3 AFE Control

Step xi Press the > ATTRIBUTES < button. Select the “AFE Control” option from the pull down menu. The AFE Control Attribute Display window appear. Press the >UPDATE< button and refer to the afeModInStatus, afeModOutStatus, afeITemperature1 and afeTemperature2 fields. Verify values are consistent with the Checklist requirements. Record the two temperature values in the NOTES section of the Checklist.

Step xii Close the AFE Control Attribute window.

Figure 7. AFE Supply Test Point Locations

Step 3.2.3 Close the AFE Supplies Attribute window.

Created on 1/26/2012

Page 12 of 22
3.4 AFE Clocks

Step xiii  Press the >ATTRIBUTES< button. Select the “AFE1 Clocks” option from the pull down menu. The AFE Clocks Attribute Display window will appear.

Step xiv In MEC window, press the >DHE CONTROL< button. Select the “Display Mode Files” option from the pull down menu. The Mode File Select window will be displayed. Scroll to the bottom of the window and select the “manualClkTest.mod” file then press the >LOAD< button. The Mode File Select window will disappear and the .mod file will be loaded and ready for use.

Step xv Press the >UPDATE< button on the AFE1 Clocks Attribute Display window. The voltages for the LOW_RAILS and HIGH_RAILS values will be displayed for each clock.

**NOTE:** The Low Rail Clock voltages are denoted with negative polarity and sequentially numerated for easy identification. For functional purposes ClkLo[0] is identified with a value of -0.50V

**NOTE:** The High Rail Clock voltages are denoted with positive polarity and sequentially numerated for easy identification. For functional purposes Clk[0] is identified with a value of +0.50V

Step xvi Enable the Clock voltages to the AFE by entering “15” in the clkEnbl field, then hit the Enter key on the keyboard. Press the >UPDATE< button on the AFE1 Clocks Attribute Display window to update the CLOCK_TELM fields for each clock.

**NOTE:** By default, the test code sets the Low Clock Rails first. Verify the Low Rails have been loaded to the AFE by observing the negative polarity values displayed on the CLOCK_TELM field for each clock.

Step xvii Measure the Low Clock Rail values on the AFE at the near side of AFE connector J1. Refer to Figure 8 for clock locations. Record the measured value of each Clock on the Manual AFE Acceptance Test Checklist where provided.

![Figure 8. AFE Clock Locations](image)

Created on 1/26/2012

Page 13 of 22
Step xviii Manually set the High Clock Rails by changing the value of the afeClkStateReg field to “0xffffffff” then, press the Enter key on the keyboard. Press the >UPDATE< button on the AFE1 Clocks Attribute Display window to update the CLOCK_TELM fields for each clock. Verify that each clock value changes polarity.

Step xix Measure the High Clock Rail values on the AFE at the near side of AFE connector J1. Refer to Figure 8 for clock locations. Record the measured value of each Clock on the Manual AFE Acceptance Test Checklist where provided.

Step xx Disable the Clock voltages to the AFE by entering “0” in the clkEnbl field, then hit the Enter key on the keyboard. Press the >UPDATE< button on the AFE1 Clocks Attribute Display window to execute the Disable command.

Verify that all clocks have been disabled on the AFE by measuring each clock value. All clocks should measure zero volts. Designate clock disable check on the Manual AFE Acceptance Test Checklist where provided.

Step xxi Test the functionality of the Global Clock enable function by entering a positive value in the afeClkHiVal[ ] field and/or a negative value in the afeClkLoVal[ ] of the AFE1 Clocks Attribute Display window.

Press the Enter key on the keyboard to set the global clock value. Press the >UPDATE< button on the AFE1 Clocks Attribute Display window to update the CLOCK_TELM fields for each clock.

**NOTE:** If the afeClkStateReg value is “-1”, the CLOCK_TELM will display the Hi Clock values.

If the afeClkStateReg value is “0”, the CLOCK_TELM will display the Lo Clock values

Verify that all clocks have been set to the Global value on the AFE by measuring each clock. All clocks should measure the same voltage. Designate Global Clock check on the Manual AFE Acceptance Test Checklist where provided.

Step xxiii Close the AFE1 Clocks Attribute Display window.

### 3.5 AFE Bias

**Step 3.5.1** Press the >ATTRIBUTES< button. Select the “AFE Bias Voltage” option from the pull down menu. The AFE Bias Voltages Attribute Display window will appear.

**Step 3.5.2** In MEC window, press the >DHE CONTROL< button. Select the “Display Mode Files” option from the pull down menu. The Mode File Select window will be displayed. Scroll to the bottom of the window and select the “manualBiasTest.mod” file then press the >LOAD< button. The Mode File Select window will disappear and the .mod file will be loaded and ready for use.
Step 3.5.3 Press the >UPDATE< button on the AFE Bias Voltages Attribute Display window. The voltages for the LOW_V_BIAS and HIGH_V_BIAS values will be displayed for each bias.

**NOTE:** The Low Bias voltages are denoted with negative polarity and sequentially numerated for easy identification. For functional purposes afe1LVBiasVal[0] is identified with a value of -0.50V

**NOTE:** The High Bias voltages are denoted with positive polarity and sequentially numerated for easy identification. For functional purposes afe1HVBiasVal[0] is identified with a value of +0.50V

Step 3.5.4 Enable the Bias voltages to the AFE by entering “15” in the biasEnbl field, then hit the Enter key on the keyboard. Press the >UPDATE< button on the AFE Bias Voltages Attribute Display window to execute the Enable command.

Step 3.5.5 Measure the Low Bias values on the AFE at the near side of AFE connector J1. Refer to Figure 8 for LV Bias locations. Record the measured value of each LV Bias on the Manual AFE Acceptance Test Checklist where provided.

Step 3.5.6 Measure the High Bias values on the AFE at the near side of AFE connector J1. Refer to Figure 8 for HV Bias locations. Record the measured value of each HV Bias on the Manual AFE Acceptance Test Checklist where provided.

Step 3.5.7 Test the functionality of the Global Positive HV Bias enable function by entering a value of “28” in the afe1HVBiasVal[ ], then hit the Enter key on the keyboard. Press the >UPDATE< button on the AFE Bias Voltages Attribute Display window to update HV_BIAS_TEL fields for each Bias.

**NOTE:** Entering a value of 28 will simultaneously test the maximum positive voltage limit for the HV Bias of the AFE.

Measure the High Bias values on the AFE. Record the measured value of each HV Bias Limit on the Manual AFE Acceptance Test Checklist where provided.

Step 3.5.8 Disable the Bias voltages to the AFE by entering “0” in the biasEnbl field, then hit the Enter key on the keyboard. Press the >UPDATE< button on the AFE Bias Voltages Attribute Display window to execute the Disable command.

Verify that all bias’ have been disabled on the AFE by measuring each LV and HV Bias values. All bias’ should measure zero volts. Designate bias disable check on the Manual AFE Acceptance Test Checklist where provided.

Step 3.5.9 In MEC window, press the >DHE CONTROL< button. Select the “Display Mode Files” option from the pull down menu. The Mode File Select window will be displayed. Scroll to the bottom of the window and select the “manualNegPolarity.mod” file then press the >LOAD< button. The Mode File Select window will disappear and the .mod file will be loaded and ready for use.
Step 3.5.10 Press the >UPDATE< button on the AFE Bias Voltages Attribute Display window. The negative polarity voltages for the HIGH_V_BIAS values will be displayed for each bias.

**NOTE:** This test will test the functionality of the HV Negative Polarity feature. As a result, the High Bias voltages are denoted with negative polarity and sequentially numerated for easy identification. For functional purposes afe1HVBiasVal[0] is identified with a value of -0.50V

Step 3.5.11 Enable the Bias voltages to the AFE by entering “15” in the biasEnbl field, then hit the Enter key on the keyboard. Press the >UPDATE< button on the AFE Bias Voltages Attribute Display window to execute the Enable command.

Step 3.5.12 Measure the negative High Bias values on the AFE. Record the measured value of each HV Bias on the Manual AFE Acceptance Test Checklist where provided.

Step 3.5.13 Test the functionality of the Global Negative HV Bias enable function by entering a value of “-28” in the afe1HVBiasVal[], then hit the Enter key on the keyboard. Press the >UPDATE< button on the AFE Bias Voltages Attribute Display window to update HV_BIAS_TEL fields for each Bias.

**NOTE:** Entering a value of -28 will simultaneously test the maximum negative voltage limit for the HV Bias of the AFE.

Measure the High Bias values on the AFE. Record the measured value of each HV Bias Limit on the Manual AFE Acceptance Test Checklist where provided.

Step 3.5.14 Return the AFE to the Positive HV Bias configuration by press the >DHE CONTROL< button in the MEC window. Select the “Display Mode Files” option from the pull down menu. The Mode File Select window will be displayed. Scroll to the bottom of the window and select the “manualPosPolarity.mod” file then press the >LOAD< button. The Mode File Select window will disappear and the .mod file will be loaded and ready for use.

Press the >UPDATE< button (as required) on the AFE Bias Voltages Attribute Display window to update HV_BIAS_TEL fields back to positive values for each Bias.

Step 3.5.14 AFE Bias Voltages Attribute Display window
3.6 AFE Video

Step 3.6.1 Press the >Attributes< button. Select the “Exposure Variables” option from the pull down menu. The Exposure Attribute Display window will appear.

Step 3.6.2 Enter the image directory Path (created in Step 3.1.3) in the imageDir Field, then hit the Enter key on the keyboard.

Enter the designated image file name, then hit the Enter key on the keyboard.

**NOTE:** The image file name should carry the serial number and conducted noise test number. For example, is AFE sn001 is under test, the image file name must be:

sn001noise1

Press the >Update< button on the Exposure Variable Attribute Display window to load the image information into the mBORG. Do not close the Exposure Attribute window.

Step 3.6.3 Press the >Attributes< button. Select the “Environment Attributes” option from the pull down menu. The Environment Attributes Attribute Display window will appear.

Verify that the dwnLdFname field has the “noise1.ucd” value entered, then press the >Update< button. Do not close the Environment Attribute window.

Step 3.6.4 In MEC window, press the >DHE Control< button. Select the “Load Current .ucd File” option from the pull down menu. The noise1.ucd file will be loaded and ready for use.

Step 3.6.5 Prepare the AFE to take an exposure sequence by enabling the sequencer in the MEC window; press the pink >Sequencer Disabled< button.

**NOTE:** The Sequencer button toggles to green and reflects a Sequencer Enabled description.

Change the value in the Number of Exposures field in the MEC window to 3.

Press the green >Start< button in the MEC window.

The mBORG will initiate the Exposure Sequence.

Step 3.6.5 Once the noise1 exposure sequence is complete, disable the Sequencer by pressing the green >Sequencer Enabled< button.

**NOTE:** The Sequencer button toggles to pink and reflects a Sequencer Disabled description.

Step 3.6.6 Return to the Exposure Attribute Display window and change the imageFile name noise1 descriptor to noise2, then hit the Enter key on the keyboard.

Press the >Update< button
Step 3.6.7 Return to the Environments Attribute Display window and change the
dwnLdFname field to “noise2.ucd”, then hit the **Enter** key on the keyboard.
Press the **UPDATE** button.

Step 3.6.8 Return to the MEC window and press the **DHE CONTROL** button. Select the
“Load Current .ucd File” option from the pull down menu. The noise2.ucd file
will be loaded and ready for use.

Step 3.6.9 Enable the Sequencer by pressing the pink **SEQUNCER DISABLED** button.

Step 3.6.10 Press the green **START** button in the MEC window.
The mBORG will initiate the Exposure Sequence.

Step 3.6.11 Once the noise2 exposure sequence is complete, disable the Sequencer by pressing
the green **SEQUNCER ENABLED** button.

Step 3.6.12 Return to the Exposure Attribute Display window and change the imageFile name
noise1 descriptor to noise3, then hit the **Enter** key on the keyboard.
Press the **UPDATE** button

Step 3.6.13 Return to the Environments Attribute Display window and change the
dwnLdFname field to “noise3.ucd”, then hit the **Enter** key on the keyboard.
Press the **UPDATE** button.

Step 3.6.14 Return to the MEC window and press the **DHE CONTROL** button. Select the
“Load Current .ucd File” option from the pull down menu. The noise3.ucd file
will be loaded and ready for use.

Step 3.6.15 Enable the Sequencer by pressing the pink **SEQUNCER DISABLED** button.

Step 3.6.16 Press the green **START** button in the MEC window.
The mBORG will initiate the Exposure Sequence.

Step 3.6.17 Once the noise3 exposure sequence is complete, disable the Sequencer by pressing
the green **SEQUNCER ENABLED** button.

Step 3.6.18 Return to the Exposure Attribute Display window and change the imageFile name
noise1 descriptor to noise4, then hit the **Enter** key on the keyboard.
Press the **UPDATE** button

Step 3.6.19 Return to the Environments Attribute Display window and change the
dwnLdFname field to “noise4.ucd”, then hit the **Enter** key on the keyboard.
Press the **UPDATE** button.

Step 3.6.20 Return to the MEC window and press the **DHE CONTROL** button. Select the
“Load Current .ucd File” option from the pull down menu. The noise4.ucd file
will be loaded and ready for use.
Step 3.6.21 Enable the Sequencer by pressing the pink \textit{SEQUNCER DISABLED} button.

Step 3.6.22 Press the green \textit{START} button in the MEC window.

The mBORG will initiate the Exposure Sequence.

Step 3.6.23 Once the noise4 exposure sequence is complete, disable the Sequencer by pressing the green \textit{SEQUNCER ENABLED} button.

Close the Exposure Variables Attribute window.

Close the Environment Attributes window.

In the MEC window, press the \textit{SHUTDOWN PAN} button.

Then press the pink \textit{EXIT SYSTEM} button.

Power down the Torrent Test Unit and remove the AFE Board from the Test Unit. Store it in the designated Inventory location.

Stage 4 AFE Electronics Performance Analysis

This testing stage analyzes data acquired about the board under test in Stage 3. This stage also allows the test operator to see the results of the analysis in the form of numerical representations as shown in Figure 9. Comparisons of analysis results with those of a known operational circuit board will aid in the investigation of any problems that may arise.

4.1 Image Data Retrieval

Step 4.1.1 Open an xterm window, if one is not already open. Navigate to the image data directory by entering the following into the command prompt:

\texttt{cd /data/AFETests} \hspace{1cm} \textit{Note the space after cd}

A listing of directories can be displayed by typing:

\texttt{ls}

Step 4.1.2 Navigate to the respective directory of the serial number for the AFE under test by typing:

\texttt{cd snxxx} \hspace{1cm} \textit{(where xxx is the appropriate serial number)}

Step 4.1.3 Verify the images are contained in the AFE serial number directory by typing:

\texttt{ls}

A total of twelve .fits files should be listed.
4.2 Preliminary Image Data Analysis

The size of the image data taken in Step 3.6 is a 1024 x 1024 region. This region is divided into four quadrants, with each quadrant representing a single AFE Video Channel. In order to better understand the individual channel regions, refer to Figure X in Appendix 1 for a visual representation of the quadrant scheme.

Several columns of each quadrant structure have been assigned as Pre-Scan pixels and will not be included in the overall noise analysis for each channel. Instead, the noise analysis will be performed on a specified coordinate boundary inside each quadrant that exclude the Pre-Scan pixels. Table 1 of Appendix 1 defines the boundary regions for each channel.

Step 4.2.1 Open another xterm window and navigate to the home directory of the mastodon PAN by typing:

```
cd /home/monsoon
```

Step 4.2.2 Open the iraf Analysis tool, by typing the following into the command prompt:

```
cl
```

Verify that the command prompt changes to:

```
ecl>
```

Step 4.2.3 Navigate to the AFE Under Test image directory by repeating Steps 4.1.1 through 4.1.3 inside the `ecl>` prompt.

Step 4.2.4 Analyze AFE Channel 1 shorted input image data by using the iraf imstat analysis tool. Execute the imstat tool by typing the following in the `ecl>` prompt:

```
ecl> imstat sn*fits[2]/[10:500,10:500]
```

The iraf tool should return a window similar to Figure 9.

![Figure 9. Typical imstat result display](image)

Step 4.2.5 Verify that the noise results are within the limits specified in Table XX of Appendix XX.
Record the MEAN and STDDEV results for Channel 1 on the Manual AFE Acceptance Test Checklist where provided.

Step 4.2.6 If the results are acceptable, proceed to analyze the remaining Channels per the designated channel regions identified in Table X of Appendix X.

Record the MEAN and STDDEV results for each channel on the Manual AFE Acceptance Test Checklist where provided.

Step 4.2.6 If the shorted input image data results are acceptable for the remaining channels, close the iraf connection by typing:

```
ecl> logout
```

### 4.3 Image Data Transfer

After preliminary imstat results are deemed acceptable, the data must be transferred to the official and secure document control folder on the `\big-boy\MNSN` disk. Transferring the data images to the secured location will enable the System Engineer to review the data and make the final determination of acceptability of the AFE under test.

Step 4.3.1 In the xterm window, navigate to the AFE Under Test image directory by repeating Steps 4.1.1 through 4.1.3.

Step 4.3.2 Establish a connection to the `\big-boy\MNSN` disk. Type:

```
sftp   monsoon@big-boy
```
Enter the monsoon password, if required
Verify that the command prompt changes to:

```
sftp>
```

Step 4.3.3 Navigate to the Torrent Document Control directory by typing:

```
sftp> cd   /MNSN/engr_Development/Torrent/DOC_CTRL/EL-08/08-0004_AFE_CCD
```
Create a directory of the serial number for the AFE under test by typing:

```
sftp> mkdir   snxxx  (where xxx is the appropriate serial number).
```

Step 4.3.4 Navigate to the respective directory of the serial number for the AFE under test by typing:

```
sftp> cd   snxxx   (where xxx is the appropriate serial number)
```

Step 4.3.5 Transfer the files from mastodon to `big-boy` by typing:

```
sftp> put   *.*
```

Step 4.3.6 Disconnect from `big-boy` by typing:

```
sftp> bye
```

The AFE Board can now be considered functional and ready for Final Acceptance. Update the applicable AFE ART document to reflect the test date and acceptability status where provided.
2.0 Appendix

2.1 AFE Channel Region Definitions

The table below defines the regions for each AFE Channel for use with the iraf Analysis imstat Tool:

<table>
<thead>
<tr>
<th>Region Coordinates</th>
<th>Channel 1</th>
<th>Channel 2</th>
<th>Channel 3</th>
<th>Channel 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>[10:500,10:500]</td>
<td>[520:1010,10:500]</td>
<td>[520:1010,520:1010]</td>
<td>[10:500,520:1010]</td>
<td></td>
</tr>
</tbody>
</table>

Table 1. AFE Channel Boundary Region Coordinates

2.2 Noise Figure Limits

The table below describes the Acceptable noise limits (in ADU) for shorted video inputs, for each of the four channels of AFE Under Test:

<table>
<thead>
<tr>
<th>LIMITS</th>
<th>MIN NOISE1</th>
<th>NOISE2</th>
<th>NOISE3</th>
<th>NOISE4</th>
<th>MAX NOISE1</th>
<th>NOISE2</th>
<th>NOISE3</th>
<th>NOISE4</th>
</tr>
</thead>
<tbody>
<tr>
<td>CH1</td>
<td>2.318</td>
<td>2.528</td>
<td>1.800</td>
<td>1.799</td>
<td>3.101</td>
<td>2.718</td>
<td>2.318</td>
<td>2.445</td>
</tr>
<tr>
<td>CH2</td>
<td>2.358</td>
<td>2.539</td>
<td>1.753</td>
<td>1.751</td>
<td>3.093</td>
<td>2.656</td>
<td>2.528</td>
<td>2.687</td>
</tr>
<tr>
<td>CH3</td>
<td>2.407</td>
<td>2.488</td>
<td>1.791</td>
<td>1.852</td>
<td>3.0106</td>
<td>2.691</td>
<td>2.627</td>
<td>2.697</td>
</tr>
<tr>
<td>CH4</td>
<td>2.300</td>
<td>2.716</td>
<td>1.718</td>
<td>1.709</td>
<td>3.356</td>
<td>3.05</td>
<td>2.708</td>
<td>2.969</td>
</tr>
</tbody>
</table>

Table 2. Noise Figure Limits