<table>
<thead>
<tr>
<th>Version</th>
<th>Date Approved</th>
<th>Sections Affected</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>2/16/12</td>
<td>All</td>
<td>Original Version</td>
</tr>
</tbody>
</table>

Created on 2/16/2012

Page 2 of 23
Table of Contents

Revision History .................................................................................................................................................2
Table of Contents ...............................................................................................................................................3
List of Figures .....................................................................................................................................................4
List of Tables ....................................................................................................................................................4
1.0 Introduction .................................................................................................................................................5
  1.1 Required Equipment .................................................................................................................................6
  1.2 Test Schedule ...........................................................................................................................................6
    Stage 1  Preparation of Documentation and Pre-Test Inspection .................................................................6
    Stage 2  LCB Board Test Setup .....................................................................................................................8
    Stage 3  LCB Testing Sequence .....................................................................................................................9
      3.1 LCB Initialization ..................................................................................................................................9
      3.2 LCB Power Checks ...............................................................................................................................11
      3.3 DHE General .......................................................................................................................................12
      3.4 PSM Control .......................................................................................................................................12
      3.5 LCB General .......................................................................................................................................12
      3.6 AFE Supply Verification .......................................................................................................................12
      3.7 AFE Clock and Bias Functionality Verification ...................................................................................13
2.0 Appendix .....................................................................................................................................................21
  2.1 LCB Programming Guide ..........................................................................................................................21
List of Figures

Figure 1. Typical LCB Board ................................................................................................................7
Figure 2. Torrent Input Ports ..................................................................................................................8
Figure 3. Fiber Link and Buffer Status ..................................................................................................9
Figure 4. mBORG Window Display ....................................................................................................10
Figure 5. MEC Pan Windows ...............................................................................................................11
Figure 6. AFE Clock Locations ..........................................................................................................14

List of Tables

Table 1 Test Description Conventions ..................................................................................................5
Table 2 AFE Voltage Locations on Mezzanine .....................................................................................13
1.0 Introduction

This document covers the testing strategy for the TORRENT Local Control Board (LCB) to take the board from post-manufacture to a fully functional state. All tests described in this document pertain to the latest hardware revision level of the subject board. The tests described here do not prove that the board under test will meet specification but do test the full functionality of the board and identify failures that may be the result of component and manufacture problems. The test procedure assumes that the tester is familiar with the use of the mBORG Engineering Console (MEC) and can execute the required commands. The tests are divided into progressive stages ranging from 1 to N. Each higher number stage uses assumptions on the board condition that requires the previous stages to have been successfully completed.

In the description for these tests, certain conventions are followed to ease comprehension. These conventions and examples of each are presented in Table 1.

<table>
<thead>
<tr>
<th>Convention</th>
<th>Example</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linux commands that are typed on a PAN xterm window</td>
<td>meckStart</td>
<td>Boldface italics</td>
</tr>
<tr>
<td>MEC Menu Options/Selections</td>
<td>“PSM_Control”</td>
<td>Character in quotes</td>
</tr>
<tr>
<td>Buttons on the Detector Head Electronics (DHE) boards or MEC console</td>
<td>&gt;startExp&lt;</td>
<td>Bold italics underlined inside &gt; &lt; symbols</td>
</tr>
<tr>
<td>Specific Board Signal Names</td>
<td>CLK1</td>
<td>All capitals</td>
</tr>
<tr>
<td>MEC attribute names</td>
<td>mcbCodeID</td>
<td>Italics</td>
</tr>
</tbody>
</table>

The result of each test will be recorded on an Acceptance Test Report Checklist, TRNT_EL_08_xxxxSNnnnn (where SNnnnn is the serial number). This file should be saved to the official document control area of the TORRENT project in the following directory: \\
big-boy\MNS\engr_Development\Torrent\DOC_CTRL\EL-08\08-0002_LCB

This file shall be deemed the official record of the test results that may be printed out and kept in the system binder and/or supplied to the end user. All entries of data shall be made as required per this test Procedure and the Acceptance Test Report Checklist.
1.1 Required Equipment

- Torrent Test Unit
- 24V Brick Power Supply
- Fiber Cable connection to a working PAN
- Personal Computer running MS Windows 2000 or Windows XP. The PC must be connected to the network with the \big-boy\MNSN disk mapped into the Windows disk structure. Required programs are Word and WinaXe which allow connections to the mBORG software.
  OR
- Personal Computer running LINUX
- Oscilloscope - Agilent MSO7034B
- Digital Multimeter –Fluke 77 or equivalent
- Xilinx USB Platform Cable Programming Module (Model DLC9G) or Equiv

1.2 Test Schedule

Stage 1 Preparation of Documentation and Pre-Test Inspection

Step 1.1.1 Locate the Assembly Record Tag (ART) for the LCB to be tested. The ART is a record of every action that has been taken on the board. AFE ARTs are located in:\big-boy\engr_Development\Torrent\DOC_CTRL\EL-07_ARTs\07-0002_LCB
Locate testing info section and insert relevant test info as required
Step 1.1.2 Using a comparison photograph or a known good board, visually inspect the board for physical damage, missing and misplaced components. Figure 1 shows a typical AFE Board. The particular board under test may not have exactly the same layout as pictured.

Figure 1. Typical LCB Board

Step 1.1.3 Note and correct any non-conformances. Save the ART record, as required.

Step 1.1.4 Locate the LCB Test Report Template. This template must be used to document the testing sequence and measured test values. This report shall be reviewed by the Project Engineer for acceptance of the overall board performance.

The LCB Test Report Template can be located in:
\big-boy\engr_Development\Torrent\DOC_CTRL\EL-07_ARTs\07-0002_LCB
Stage 2  LCB Board Test Setup

Step 2.1.1 Locate the Torrent Test Unit and remove the Top Cover and all PCBs present in the Controller (if required), except for the Power Supply Board. Insert the LCB under test into the slot of the Power Supply Board. Secure the newly inserted LCB to the bracket holding the blue guide rails by using the original hardware and fiberglass spacer for each bracket. Connect the Heat Exchanger Fan connector to J11 of the LCB. See Figure 1.

Step 2.1.2 Locate the Test 24V Brick Power Supply and connect it to the Power Port on the Torrent Test Unit. See Figure 2.

Figure 2. Torrent Input Ports
Step 2.1.3  Remove the Fiber Optic Cable module from the Test Unit LCB and insert into LCB Under Test. Connect the Fiber Optic Cable into LCB Under Test Fiber Optic Port. See Figure 2.

Step 2.1.4  Locate the Xilinx USB Platform Cable Programming Module and insert the Grey Ribbon Cable into the JTAG Connector, J3 of the LCB Under Test.  Connect the other Black USB end to the USB port on the Test Station Computer.

Stage 3  LCB Testing Sequence

3.1 LCB Initialization

Step 3.1.1  Turn on Test Unit by pressing and holding the Power Button for TWO seconds then release. Successful Test Unit power up is achieved by verifying that the: Green LED Power Button illuminates, fan blower turn on and Red LED status lights illuminate on the RS244 LCB Connectors. See Figure 2.

Step 3.1.2  Program the LCB EEPROM using the procedure outlined in Appendix 1.

Step 3.1.3  Carefully install the test Unit Mezzanine to the LCB Under Test at appropriate location.

Step 3.1.4  Re-energize the Test Unit by pressing and holding the Power Button for TWO seconds then release.

Open one xterm window on the PAN. In the first xterm window, type fs0 and look at the fiber link status. The status will probably show data in the receive FIFO buffer and should show the DHE to be in reset mode by having the dir(ection) bit true in the IO register (i=01110). The status command should return something similar to the following:

<table>
<thead>
<tr>
<th>FibreXtreme (SL) Monitor (sl_mon) rev. 3.02 (2003/10/06)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Driver: rev. b2-835455:776764 for Linux with API rev. 2.1</td>
</tr>
<tr>
<td>Hardware: unit/bus/slot 0/1/4 - SL100 (D64) Firm. 1C.13 (1C.13) for 5.0V PCI</td>
</tr>
<tr>
<td>Link Control Register (CSR 0x08) = 0x37</td>
</tr>
<tr>
<td>Link Status Register (CSR 0x0c) = 0x200 Link is UP</td>
</tr>
<tr>
<td>FPDP Flags Register (CSR 0x10) = 0x200 NR.D.P2.P1.S:</td>
</tr>
<tr>
<td>i=01110 o=00000</td>
</tr>
<tr>
<td>FIFO Threshold Register (CSR 0x14) = 0x0 Int.thr. = 0x0</td>
</tr>
<tr>
<td>Data count = 0xE75D (59229) bytes</td>
</tr>
<tr>
<td>Link (and other) Errors = 3</td>
</tr>
<tr>
<td>Configurable parameters: Loop Configuration: 0 (Point-to-Point)</td>
</tr>
<tr>
<td>Max Timeout: 600000 (600000 ms) Flow Control: 0 (NO)</td>
</tr>
<tr>
<td>1 (YES) Halt on link error: 1 (YES) Allow Queuing on link error:</td>
</tr>
</tbody>
</table>

Figure 3.  Fiber Link and Buffer Status

Created on 2/16/2012

Page 9 of 23
Step 3.1.5 Use the command \texttt{fc0} to clear the read buffer. Repeat the \texttt{fc0} command as required to clear any link errors. Confirm with the status command that the read FIFO buffer is now empty (\textit{Data count} = \texttt{0x0 (0) bytes}) and that no link errors persist.

Step 3.1.6 In the xterm window, start the PAN software and the mBORG using the command:

\begin{verbatim}
runManual mastodon &
\end{verbatim}

The mBORG Engineering Console (MEC) and mBORG Welcome windows will be displayed as shown in Figure 4.

\begin{figure}
\centering
\includegraphics[width=\textwidth]{mBORG_window_display.png}
\caption{mBORG Window Display}
\end{figure}
Step 3.1.7 Press the $\texttt{CONNECT}$ button on the MEC. The four pan Windows will be displayed as shown in Figure 5.

![Image of MEC Pan Windows]

Figure 5. MEC Pan Windows

Step 3.1.8 Press the $\texttt{DHE CONTROL}$ button and execute a Reset DHE sequence by selecting “Reset DHE” from the pull down menu.

Step 3.1.9 Press the $\texttt{DHE CONTROL}$ button again and execute an Initialize DHE sequence by selecting “Initialize DHE” from the pull down menu.

3.2 LCB Power Checks

Step 3.2.1 Measure the LCB Supply voltages at their designated test points (per the Checklist). Record the results on the Manual LCB Acceptance Test Checklist where provided.
3.3 DHE General

Step 3.3.1 Press the >ATTRIBUTES< button. Select the “DHE General” option from the pull down menu. The DHE General Attribute Display window will appear. Press the >UPDATE< button and refer to the VccAmps, watchDogEnable, sysCodeID, watchDogPeriod and vFanTemperature fields. Record the readings on the Manual LCB Acceptance Test Checklist where provided.

Step 3.3.2 Close the DHE General Attribute window.

3.4 PSM Control

Step 3.4.1 Press the >ATTRIBUTES< button. Select the “PSM_Control” option from the pull down menu. The PSM Control Attribute Display window will appear. Press the >UPDATE< button and refer to the psmTemperature1, psm Temperature2, vana (+/-) servo, and vcb (+/-) servo fields. Record the readings on the Manual LCB Acceptance Test Checklist where provided.

Step 3.4.2 Close the PSM Control Attribute window.

3.5 LCB General

Step 3.5.1 Press the >ATTRIBUTES< button. Select the “LCB General” option from the pull down menu. The LCB General Attribute Display window will appear. Press the >UPDATE< button and refer to the lcbCodeId, lcbModuleID, lcbTemperature1 and lcbTemperature2 fields. Record the readings on the Manual LCB Acceptance Test Checklist where provided.

Step 3.5.2 Close the LCB General Attribute window.

3.6 AFE Supply Verification

Step 3.6.1 Press the >ATTRIBUTES< button. Select the “AFE Supplies” option from the pull down menu. The AFE SuppliesAttribute Display window will appear. Press the >UPDATE< button and refer to the vhv (+/-), vcb (+/-) and vana (+/-) voltage fields. Record the readings on the Manual LCB Acceptance Test Checklist where provided.
Step 3.6.2 Verify the AFE Supply readings by directly measuring these voltages at the Mezzanine Board of the Test Unit.

The AFE Supply voltage measurements must be made for both AFE1 and AFE2. Refer to Table 1 below for locations of AFE Supply voltages.

<table>
<thead>
<tr>
<th>AFE1 Voltage Mezz Location</th>
<th>AFE2 Voltage Mezz Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>vhv +</td>
<td>Q7 (2)</td>
</tr>
<tr>
<td>vhv -</td>
<td>Q5 (1)</td>
</tr>
<tr>
<td>vcb +</td>
<td>Q16 (2)</td>
</tr>
<tr>
<td>vcb -</td>
<td>Q12 (1)</td>
</tr>
<tr>
<td>vana +</td>
<td>Q18 (2)</td>
</tr>
<tr>
<td>Vana -</td>
<td>Q15 (1)</td>
</tr>
</tbody>
</table>

Table 2  AFE Voltage Locations on Mezzanine

Step 3.6.3 Close the AFE Supplies Attribute window

Step 3.6.4 Turn OFF the Test Unit by pressing and holding the Power Button for TWO seconds then release

3.7 AFE Clock and Bias Functionality Verification

Step 3.7.1 Carefully install the Test Unit AFE Board into the AFE1 Slot (at XA1J1 and XA1J2) of the LCB Under Test.

Step 3.7.2 Re-energize the Test Unit by pressing and holding the Power Button for TWO seconds then release.

Step 3.7.3 Press the >ATTRIBUTES< button. Select the “AFE1 Clocks” option from the pull down menu. The AFE1 Clocks Attribute Display window will appear.

Step 3.7.4 In MEC window, press the >DHE CONTROL< button. Select the “Display Mode Files” option from the pull down menu. The Mode File Select window will be displayed. Scroll to the bottom of the window and select the “manualClkTest.mod” file then press the >LOAD< button. The Mode File Select window will disappear and the .mod file will be loaded and ready for use.
Step 3.7.5 Press the \texttt{UPDATE} button on the AFE1 Clocks Attribute Display window. The set voltages for the \texttt{LOW\_RAILS} and \texttt{HIGH\_RAILS} values will be displayed for each clock.

\textbf{NOTE:} The Low Rail Clock voltages are denoted with negative polarity and sequentially numerated for easy identification. For functional purposes ClkLo[0] is identified with a value of -0.50V

\textbf{NOTE:} The High Rail Clock voltages are denoted with positive polarity and sequentially numerated for easy identification. For functional purposes Clk[0] is identified with a value of +0.50V

Step 3.7.6 Enable the Clock voltages to the AFE by entering “15” in the clkEnbl field, then hit the \texttt{Enter} key on the keyboard. Press the \texttt{UPDATE} button on the AFE1 Clocks Attribute Display window to update the CLOCK\_TELM fields for each clock.

\textbf{NOTE:} By default, the test code sets the Low Clock Rails first. Verify the Low Rails have been loaded to the AFE by observing the negative polarity values displayed on the CLOCK\_TELM field for each clock.

Step 3.7.7 Measure the Low Clock Rail values on the AFE at the near side of AFE connector J1. Refer to Figure 8 for clock locations.

Verify that each Clock location reflects the Low Clock Telemetry Reading on the AFE1 Clock Attributes Display window.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{afe_clock_locations.png}
\caption{AFE Clock Locations}
\end{figure}

Step 3.7.8 Manually set the High Clock Rails by changing the value of the afeClkStateReg field to “0xffffffff” then, press the \texttt{Enter} key on the keyboard. Press the \texttt{UPDATE} button on the AFE1 Clocks Attribute Display window to update the CLOCK\_TELM fields for each clock. Observe that each clock telemetry value changes polarity.
Step 3.7.9  Measure the High Clock Rail values on the AFE at the near side of AFE connector J1. Refer to Figure 8 for clock locations.

Verify that each Clock location reflects the High Clock Telemetry Reading on the AFE1 Clock Attributes Display window.

Step 3.7.10 Disable the Clock voltages to the AFE by entering “0” in the clkEnbl field, then hit the Enter key on the keyboard. Press the >UPDATE< button on the AFE1 Clocks Attribute Display window to execute the Disable command.

Verify that all clocks have been disabled on the AFE by measuring each clock value. All clocks should measure zero volts.

Step 3.7.11 Test the functionality of the Global Clock enable function by entering a positive value in the afeClkHiVal[ ] field and/or a negative value in the afeClkLoVal[ ] of the AFE1 Clocks Attribute Display window.

Press the Enter key on the keyboard to set the global clock value. Press the >UPDATE< button on the AFE1 Clocks Attribute Display window to update the CLOCK_TELM fields for each clock.

NOTE: If the afeClkStateReg value is “-1”, the CLOCK_TELM will display the Hi Clock values.

If the afeClkState Reg value is “0”, the CLOCK_TELM will display the Lo Clock values

Verify that all clocks have been set to the Global value on the AFE by measuring each clock. All clocks should measure the same voltage.

Step 3.7.12 Record that all the LCB Under Test satisfactorily performs all the Clock Functions as checked above. Also record that all the Clock Voltage polarities were verified by measurement. Record as required on the Manual AFE Acceptance Test Checklist where provided

Step 3.7.13 Close the AFE1 Clocks Attribute Display window.

Step 3.7.14 Press the >ATTRIBUTES< button. Select the “AFE Bias Voltage” option from the pull down menu. The AFE Bias Voltages Attribute Display window will appear.

Step 3.7.15 In MEC window, press the >DHE CONTROL< button. Select the “Display Mode Files” option from the pull down menu. The Mode File Select window will be displayed. Scroll to the bottom of the window and select the “manualBiasTes.mod” file then press the >LOAD< button. The Mode File Select window will disappear and the .mod file will be loaded and ready for use.
Step 3.7.16. Press the >UPDATE< button on the AFE Bias Voltages Attribute Display window. The set voltages for the LOW_V_BIAS and HIGH_V_BIAS values will be displayed for each bias an AFE1 and AFE2 slots

**NOTE:** The Low Bias voltages are denoted with negative polarity and sequentially numerated for easy identification. For functional purposes afe1LVBiasVal[0] is identified with a value of -0.50V

**NOTE:** The High Bias voltages are denoted with positive polarity and sequentially numerated for easy identification. For functional purposes afe1HVBiasVal[0] is identified with a value of +0.50V

Step 3.7.17 Enable the Bias voltages to the AFE1 by entering “15” in the biasEnbl field, then hit the Enter key on the keyboard. Press the >UPDATE< button on the AFE Bias Voltages Attribute Display window to execute the Enable command.

Step 3.7.18 Measure the Low and High Bias values on the AFE at the near side of AFE connector J1. Refer to Figure 8 for Bias locations

Verify that each Bias location reflects the Low V Bias and High V Bias Telemetry reading on the AFE BiasAttributes Display window.

Step 3.7.19 Disable the Bias voltages to the AFE by entering “0” in the biasEnbl field, then hit the Enter key on the keyboard. Press the >UPDATE< button on the AFE Bias Voltages Attribute Display window to execute the Disable command.

Verify that all bias’ have been disabled on the AFE by measuring each LV and HV Bias values. All bias’ should measure zero volts.

Step 3.7.20 In MEC window, press the >DHE CONTROL< button. Select the “Display Mode Files” option from the pull down menu. The Mode File Select window will be displayed. Scroll to the bottom of the window and select the “manualNegPolarity.mod” file then press the >LOAD< button. The Mode File Select window will disappear and the .mod file will be loaded and ready for use.

Step 3.7.21 Press the >UPDATE< button on the AFE Bias Voltages Attribute Display window. The negative polarity set voltages for the HIGH_V_BIAS values will be displayed for each bias.

**NOTE:** This test will test the functionality of the HV Negative Polarity feature. As a result, the High Bias voltages are denoted with negative polarity and sequentially numerated for easy identification. For functional purposes afe1HVBiasVal[0] is identified with a value of -0.50V

Step 3.7.21 Enable the Bias voltages to the AFE1 by entering “15” in the biasEnbl field, then hit the Enter key on the keyboard. Press the >UPDATE< button on the AFE Bias Voltages Attribute Display window to execute the Enable command.

Step 3.7.22 Measure the negative High Bias values on the AFE.

Verify that each HV Bias location reflects the new Negative Polarity Voltage Telemetry reading on the AFE BiasAttributes Display window.
Step 3.7.23 Test the functionality of the Global Negative HV Bias enable function by entering a value of “-28” in the afe1HVBiasVal[], then hit the Enter key on the keyboard. Press the >UPDATE< button on the AFE Bias Voltages Attribute Display window to update HV_BIAS_TEL fields for each Bias.

**NOTE:** Entering a value of -28 will simultaneously test the maximum negative voltage limit for the HV Bias of the AFE.

Measure the High Bias values on the AFE. Verify that each HV Bias location reflects the new Negative Polarity Voltage Telemetry reading on the AFE BiasAttributes Display window.

Step 3.7.24 Return the AFE to the Positive HV Bias configuration by press the >DHE CONTROL< button in the MEC window. Select the “Display Mode Files” option from the pull down menu. The Mode File Select window will be displayed. Scroll to the bottom of the window and select the “manualPosPolarity.mod” file then press the >LOAD< button. The Mode File Select window will disappear and the .mod file will be loaded and ready for use.

Press the >UPDATE< button (as required) on the AFE Bias Voltages Attribute Display window to update HV_BIAS_TEL fields back to positive values for each Bias.

Step 3.7.25 Turn OFF the Test Unit by pressing and holding the Power Button for TWO seconds then release.

Step 3.7.26 Record that all the LCB Under Test satisfactorily performs all the Bias Functions as checked above. Also record that all the Bias Voltage polarities were verified by measurement. Record as required on the Manual AFE Acceptance Test Checklist where provided.

Step 3.7.27 Carefully remove the Test Unit AFE Board and install it into the AFE2 Slot (at XA2J1 and XA2J2) of the LCB Under Test.

Step 3.7.28 Re-energize the Test Unit by pressing and holding the Power Button for TWO seconds then release.

Step 3.7.29 Press the >ATTRIBUTES< button. Select the “AFE2 Clocks” option from the pull down menu. The AFE2 Clocks Attribute Display window will appear.

Step 3.7.30 In MEC window, press the >DHE CONTROL< button. Select the “Display Mode Files” option from the pull down menu. The Mode File Select window will be displayed. Scroll to the bottom of the window and select the “manualClkTest.mod” file then press the >LOAD< button. The Mode File Select window will disappear and the .mod file will be loaded and ready for use.
Step 3.7.31  Press the >UPDATE< button on the AFE1 Clocks Attribute Display window. The set voltages for the LOW_RAILS and HIGH_RAILS values will be displayed for each clock.

**NOTE:** The Low Rail Clock voltages are denoted with negative polarity and sequentially numerated for easy identification. For functional purposes ClkLo[0] is identified with a value of -0.50V

**NOTE:** The High Rail Clock voltages are denoted with positive polarity and sequentially numerated for easy identification. For functional purposes Clk[0] is identified with a value of +0.50V

Step 3.7.32  Enable the Clock voltages to the AFE by entering “240” in the clkEnbl field., then hit the Enter key on the keyboard. Press the >UPDATE< button on the AFE2 Clocks Attribute Display window to update the CLOCK_TELM fields for each clock.

**NOTE:** By default, the test code sets the Low Clock Rails first. Verify the Low Rails have been loaded to the AFE by observing the negative polarity values displayed on the CLOCK_TELM field for each clock.

Step 3.7.33  Measure the Low Clock Rail values on the AFE at the near side of AFE connector J1.

Verify that each Clock location reflects the Low Clock Telemetry Reading on the AFE1 Clock Attributes Display window.

Step 3.7.34  Manually set the High Clock Rails by changing the value of the afeClkStateReg field to “0xffffffff” then, press the Enter key on the keyboard. Press the >UPDATE< button on the AFE2 Clocks Attribute Display window to update the CLOCK_TELM fields for each clock. Observe that each clock telemetry value changes polarity.

Step 3.7.35  Measure the High Clock Rail values on the AFE at the near side of AFE connector J1. Refer to Figure 8 for clock locations.

Verify that each Clock location reflects the High Clock Telemetry Reading on the AFE2 Clock Attributes Display window.

Step 3.7.36  Disable the Clock voltages to the AFE by entering “0” in the clkEnbl field., then hit the Enter key on the keyboard. Press the >UPDATE< button on the AFE2 Clocks Attribute Display window to execute the Disable command.

Verify that all clocks have been disabled on the AFE by measuring each clock value. All clocks should measure zero volts.
Step 3.7.37 Test the functionality of the Global Clock enable function by entering a positive value in the afeClkHiVal[] field and/or a negative value in the afeClkLoVal[] of the AFE2 Clocks Attribute Display window.

Press the **Enter** key on the keyboard to set the global clock value. Press the **>UPDATE<** button on the AFE1 Clocks Attribute Display window to update the CLOCK_TELM fields for each clock.

**NOTE:** If the afeClkStateReg value is “-1”, the CLOCK_TELM will display the Hi Clock values.

If the afeClkStateReg value is “0”, the CLOCK_TELM will display the Lo Clock values.

Verify that all clocks have been set to the Global value on the AFE by measuring each clock. All clocks should measure the same voltage.

Step 3.7.38 Record that all the LCB Under Test satisfactorily performs all the Clock Functions as checked above. Also record that all the Clock Voltage polarities were verified by measurement. Record as required on the Manual AFE Acceptance Test Checklist where provided.

Step 3.7.39 Close the AFE2 Clocks Attribute Display window.

Step 3.7.40 Press the **>ATTRIBUTES<** button. Select the “AFE Bias Voltage” option from the pull down menu. The AFE Bias Voltages Attribute Display window will appear.

Step 3.7.41 In MEC window, press the **>DHE CONTROL<** button. Select the “Display Mode Files” option from the pull down menu. The Mode File Select window will be displayed. Scroll to the bottom of the window and select the “manualBiasTest.mod” file then press the **>LOAD<** button. The Mode File Select window will disappear and the .mod file will be loaded and ready for use.

Step 3.7.42 Press the **>UPDATE<** button on the AFE Bias Voltages Attribute Display window. The set voltages for the LOW_V_BIAS and HIGH_V_BIAS values will be displayed for each bias an AFE1 and AFE2 slots.

**NOTE:** The Low Bias voltages are denoted with negative polarity and sequentially numerated for easy identification. For functional purposes afe1LVBiasVal[0] is identified with a value of -0.50V

**NOTE:** The High Bias voltages are denoted with positive polarity and sequentially numerated for easy identification. For functional purposes afe1HVBiasVal[0] is identified with a value of +0.50V

Step 3.7.43 Enable the Bias voltages to the AFE2 by entering “240” in the biasEnbl field, then hit the **Enter** key on the keyboard. Press the **>UPDATE<** button on the AFE Bias Voltages Attribute Display window to execute the Enable command.
Step 3.7.44 Measure the Low and High Bias values on the AFE at the near side of AFE connector J1.

Verify that each Bias location reflects the Low V Bias and High V Bias Telemetry reading on the AFE Bias Attributes Display window.

Step 3.7.45 Disable the Bias voltages to the AFE by entering “0” in the biasEnbl field, then hit the Enter key on the keyboard. Press the UPDATE button on the AFE Bias Voltages Attribute Display window to execute the Disable command.

Verify that all bias’ have been disabled on the AFE by measuring each LV and HV Bias values. All bias’ should measure zero volts.

Step 3.7.46 Record that all the LCB Under Test satisfactorily performs all the Bias Functions as checked above. Also record that all the Bias Voltage polarities were verified by measurement. Record as required on the Manual AFE Acceptance Test Checklist where provided.

Step 3.7.47 Turn OFF the Test Unit by pressing and holding the Power Button for TWO seconds then release.

At this time the LCB testing sequence is complete. Exit the mBORG and save the LCB Acceptance Test Checklist in the appropriate document control folder. Power OFF the Torrent Test Unit and remove the LCB from the Test Unit. Store the board in the designated Inventory location.
2.0 Appendix

2.1 LCB Programming Guide

Step 2.1 Open the iMPACT programming tool.

Step 2.2 Initialize the JTAG chain by selecting “Initialize Chain” from the FILE drop menu in the Main Window Toolbar. The “Assign New Configuration File” window will appear.

Step 2.3 Navigate to the latest Firmware Code Folder

Select the latest .mcs file and click Open

If the Select Device Part Name window appears, select “xcf32p” from the dropdown menu and click OK.

Step 2.4 Click on the Bypass button to bypass the programming of the xc5vl Device.
Step 2.5  The Device Programming Properties window will appear after the above step.

Note: the Properties shall be set for the Device 1 (PROM2, xcf32p) only

Make sure that ONLY the following boxes are checked:
  Verify
  Erase the Entire Device
  Parallel mode
  During Configuration: PROM is slave

Click “Apply”, then “OK”

Step 2.6  Right-Click on the xcf32p device icon and select Load Configuration Window from the menu.

Select Load Revision “0” from the Configuration revision window and click “OK”.

Step 2.7  Right-Click on the xcf32p device icon and select Set Erase Properties from the menu.

Make sure that ONLY the following boxes are checked:
  Erase Entire Device

Click “Apply”, then “OK”

Step 2.8  Right-Click on the xcf32p device icon and select Set Erase Properties from the menu.

Select “Program” from the menu. This command will begin the programming sequence.

Note: Programming will complete after several minutes. Do not interrupt the Progress Dialog process.

Step 2.9  Once the programming sequence is complete, reboot the LCB under test. Turn OFF the Test Unit by pressing and holding the Power Button for TWO seconds then release.

Wait a few seconds, then re-energize the LCB Under Test by pressing and holding the Power Button for TWO seconds then release.

Note: Fan speed will be slower than Pre Programmed state.
Step 3.0 Right-Click on the xcf32p device icon and select Get Device Checksum from the menu.

The checksum must match that of the latest Firmware read back. Record the Checksum value on the ART for the LCB under test.

Step 3.1 Right-Click on the xc5vlx50t device icon and select Get Device Signature/Usercode from the menu.

The Usercode must match that of the latest Firmware read back. Record the Usercode value on the ART for the LCB under test.

Step 3.2 Turn OFF the Test Unit by pressing and holding the Power Button for TWO seconds then release.

Step 3.3 Close the iMPACT tool.

Note: After closing the iMPACT tool, the exit window will appear asking about saving the project file before exit. Click “NO”, as the project must not be saved.

Return to the Testing Sequence and proceed with Step 3.1.3