MONSOON
TORRENT DHE Architecture

DHE Architecture Document
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## Revision History

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<th>Version</th>
<th>Date Approved</th>
<th>Sections Affected</th>
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<td>1.0</td>
<td>9/03/2005</td>
<td>All</td>
<td>Initial draft release - Moore</td>
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<td>2.0</td>
<td>4/13/2006</td>
<td>All</td>
<td>Changes reflect peer revision of requirements</td>
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<td>2.1</td>
<td>11/06/2006</td>
<td>All</td>
<td>Changes reflect further detailed design studies of VIS front end design</td>
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<td>3.0</td>
<td>06/28/2007</td>
<td>All</td>
<td>Revision of requirements after preliminary design.</td>
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<td>5.0</td>
<td>11/13/2009</td>
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<td>Updated document to reflect current state of Torrent project deliverables</td>
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Introduction
This document details the technical requirements for the hardware module of a generic replacement detector controller using the MONSOON architectural model. The purpose of this module is to replace existing detector controller hardware currently used in operational instrumentation where the controller has become obsolete or difficult to maintain.

1. Project working title: TORRENT

2. Area of application:
   2.1. This self contained detector controller shall have sufficient functionality to replace actual detector controllers in use through the astronomical community without compromising existing performance.

3. Advantage / motivation:
   3.1. Replace unreliable or high maintenance hardware.
   3.2. Replace hardware that cannot be repaired because of obsolete components.
   3.3. Unify detector controller architectures to reduce maintenance burden.
   3.4. Applied to new instrumentation without risk of ‘single source’ components.

4. Generic qualities:
   4.1. The application of the controller to specific functionality shall be through selection of a board suite, hardware configuration, and ‘runtime’ configuration options. The hardware assembly shall be called the Detector Head Electronics (DHE) package. Current plans for board suite selection for the DHE are:
      4.1.1. Generic Local Control Board.
      4.1.2. N Channel CCD Analog Front End board.
      4.1.3. P Channel CCD Analog Front End board.
      4.1.4. IR Analog Front End board.
      4.1.5. Power supply board.
      4.1.6. Utility Board (Temperature control, Shutter).
      4.1.7 Preamp board (or Current Source board for IR).
   4.2. The cost to purchase shall be consistent to the required capabilities i.e. cost should scale with number of video channels, etc. Baseline cost for a four channel VIS system is $10k
   4.3. The controller hardware will be compatible with existing Pixel Acquisition Node (PAN) hardware and software.
   4.4. Support for card serial numbers, self-configuration, and self-calibration using expanded NOAO software suite..
   4.5. Support for comprehensive telemetry sensing.
   4.6. Support for card temperature sensing.
5. Specific hardware capabilities – All Detectors:

5.1. Sequencer control:
5.1.1. Timing resolution: 25 ns.
5.1.2. Pattern memory store size: >1000 pattern values.
5.1.3. Sequencer code store size: > 1000 code values.

5.2. PAN/DHE communications:
5.2.1. Serial FPDP fiber port @ 1.0625 Gbps (Systran compatible).
5.2.2. 100/1000BaseT Ethernet with TCP/IP
5.2.3. Onboard image buffer, DDR DRAM - 256Mbytes.

5.3. Auxiliary Functions.
5.3.1. Support for shutter control via optical isolated open collector output.
5.3.2. Two optically isolated inputs for shutter position monitor function
5.3.3. Support for pre-flash led control via optical isolated current source output.
5.3.4. Support for single channel temperature control with set point control via DAC and linear current sink output @ max 5 Watts.
5.3.5. Ability to isolate all clock and bias signals from detector via electronic switches. Detector safety interlock on principle power supply availability and health.
5.3.6. Voltage telemetry data functions for all clocks, biases, video offsets, power supply voltages, and references.
5.3.7. Temperature control output current monitor.
5.3.8. Telemetry data function for temperature control temperature, plus one spare channel. Supplied with 10/50µa current sources for two diodes or PT100 sensors.
5.3.9. Detection for PAN disconnect with detector idle protection plan.

5.4. Power, size, and weight.
5.4.1. DHE Primary voltage supply: External inline 24VDC 60W Medical grade power supply.
5.4.2. DHE Power dissipation: < 30 Watts for maximum system.
5.4.3. DHE size: As small as possible consistent with packaging and sufficient power dissipation factors. Baseline dimensions are 195mm x 135mm x 315mm (WxHxL) for the DHE package.
5.4.4. DHE weight: As light as possible consistent with ruggedness for deployment.

6. Specific hardware capabilities – VIS Detectors:
6.1. Video input: N and P Channel CCD AFE
6.1.1. Number of input channels: 4 to 8 in increments of 4.
6.1.2. Sensitivity of input channels: 0.5 µVolt => 10.0 µVolt / ADU.
6.1.3. Video input type shall be single ended AC coupled with characteristic source impedance termination.
6.1.4. Controller noise contribution: < 2 ADU rms @ 100Kpix/sec/chan with 2K Ohm source impedance and 2 μVolt / ADU gain.
6.1.5. Conversion dynamic range shall be 18-bit with no missing codes.
6.1.6. The maximum conversion rate shall be 500 kpix/channel/sec.

6.2. Clock voltage output: N and P Channel CCD AFE
6.2.1. Number of clocks: 16 per 4 video inputs in 4 groups of 4.
6.2.2. Clock voltage range is ± 15V swing @ 30 ma peak.
6.2.3. Clock voltage setting resolution: 12 bits.
6.2.4. Clock 90% swing rise/fall time: Minimum 70 ns, adjustable slope.
6.2.5. Max ripple, overshoot and noise: Critical damped to limit overshoot to < 0.01% of value. Ripple and noise < 5 mv.

6.3. Bias voltage output: N and P Channel CCD AFE
6.3.1. Number of biases: 16 per 4 video inputs in 4 groups of 4.
6.3.2. Bias voltage ranges:
   6.3.2.1. Low Voltage Biases: ± 15V@ 25ma.
   6.3.2.2. High Voltage Biases: Unipolar 0 Volts to +30 Volts @ 25mA or -30 Volts to 0 Volts @ 25 mA.
6.3.3. Bias voltage setting resolution: 12 bits.
6.3.4. Max ripple, overshoot and noise: 0.001% of value or 20 μVolts rms.

7. Specific hardware capabilities – IR Detectors:
7.1. Video input: N and P Channel ROIC IR AFE
7.1.1. Number of input channels: 16 to 32 in increments of 16.
7.1.2. Sensitivity of input channels: 4.0 µVolt => 40.0 µVolt / ADU.
7.1.3. Video input type shall be single ended DC, coupled with optional current source compliant to detector max DC offset voltage.
7.1.4. Video common mode DC signal: +/- 6 Volts.
7.1.5. Controller noise contribution: < 1.7 ADU rms @ 800Kpix/sec/chan with 2K Ohm source impedance and 4 μVolt / ADU gain.
7.1.6. Conversion dynamic range shall be 16-bit with no missing codes.
7.1.7. The maximum conversion rate shall be 1000 Kpix/channel/sec.
7.1.8. There shall be provision for digital averaging @ 1000Kpix data rate for up to 64 samples.
7.1.9. There shall be provision for co-addition of 1024 x 1024 pixel images up to 16 deep.

7.2. Clock voltage output: N and P Channel ROIC IR AFE
7.2.1. Number of clocks: 16 per 16 video inputs, in 1 group.
7.2.2. Clock voltage range: Biplolar +/-8.0 Volts @ 30 ma peak.
7.2.3. Clock voltage setting resolution: 12 bits.
7.2.4. Clock 90% swing rise/fall time: Minimum 50 ns, adjustable slope.
7.2.5. Max ripple, overshoot and noise: Critical damped to limit overshoot to < 0.01% of value. Ripple and noise < 200 μv.
7.3. **Bias voltage output**: N and P Channel ROIC IR AFE
   7.3.1. Number of biases: 12 per 16 video inputs.
   7.3.2. Bias voltage ranges:
      5.3.2.1. Range 1: Bipolar +/-8.0 Volts @ 25ma.
      5.3.2.2. Range 2: Unipolar 0 Volts => +8.0 Volts @ 25ma.
      5.3.2.3. Range 3: Unipolar –8.0 Volts => 0 Volts @ 25ma.
   7.3.3. Bias voltage setting resolution: 12 bits.
   7.3.4. Max ripple, overshoot and noise: 0.001% of value or 20 µVolts rms.

8. **Project lifecycle**:
   Figure 1 shows the relative timing of the project lifecycle.

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**Figure 1 - Project lifecycle phases (calendar years)**

8.1. The product shall use generic electronic components to achieve the functionality wherever possible. This will maximize the useful operational life of the controller by reducing the risk of component obsolescence.

8.2. The product shall minimize the total number and types of electronic components used in the design to reduce the risk of component failure. Conservative design practice and quality component selection will be used to reduce stress on the electrical components.

8.3. The product shall utilize the layered architectural model of MONSOON. This will relieve obsolescence management tasks by defining all modules (Software/firmware/hardware/mechanical) within well defined boundaries described by the interface control documents. This allows renovation of obsolescent components by module replacement without disturbing other aspects of the system function.

9. **Project deliverables**:
Each delivered product shall consist of three packages as described below:

9.1. **Generic hardware and software package**
   9.1.1. One PAN Software package for installation in a LINUX environment.
   9.1.2. One PAN interface card for the DHE communications link (if required).
   9.1.3. One PAN to DHE communications link cable or fiber (10mtr or custom length).
9.1.4. One DHE Chassis Assembly.
9.1.5. One DHE Local Control Board (LCB).
9.1.6. One Analog Front End (AFE) board - detector type specific.
9.1.7. One power supply board.
9.1.8. One inline power supply with mating connector for the DHE.
9.1.9. One firmware package - detector type specific.
9.1.10. One documentation package including calibration and test records.

9.2. Detector specific configuration package.
   9.2.1. Detector specific software library package.
   9.2.2. Additional analog front end board (if required).
   9.2.3. DHE to detector plate cabling.
   9.2.5. Detector specific sequencer control program (note 1).
   9.2.6. Detector specific PAN configuration package (notes 1 & 2).
   9.2.7. Detector specific documentation package.

Which shall be one of the following classes of support:
   9.3.1. Basic MONSOON function support for a fixed number of hours.
   9.3.2. Blanket technical support for operational and functional aspects of
           the MONSOON controller only.
   9.3.3. Detector specific optimization and commissioning support (note 3).

Notes:
1. The sequencer control program and configuration package is intended to
   emulate current or specified detector operating environments only.
2. The configuration package is offered as a starting point for detector
   optimization. It does not guarantee optimum detector performance with the
   controller.
3. At this level of support the product become a turnkey, detector optimized
   system.